Voltage Source Multilevel Inverters With Reduced Device Count: Topological Review and Novel Comparative Factors

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***Abstract*—Multilevel inverters (MLIs) have gained increasing interest for advanced energy-conversion systems due to their features of high-quality produced waveforms, modularity, transformerless operation, voltage, and current scalability, and fault-tolerant operation. However, these merits usually come with the cost of a high number of components. Over the past few years, proposing new MLIs with a lower component count has been one of the most active topics in power electronics. The first aim of this article is to update and summarize the recently developed multilevel topologies with a reduced component count, based on their advantages, disadvantages, construction, and specific applications. Within the framework, both single-phase and three-phase topologies with symmetrical and asymmetrical operations are taken into consideration via a detailed comparison in terms of the used component count and type. The second objective is to propose a comparative method with novel factors to take component ratings into account. The effectiveness of the proposed method is verified by a comparative study.**

***Index Terms*—Asymmetric operation, comparison factor, component for each level (CEL), dc–ac converter, multilevel inverter (MLI), single-phase, symmetric operation, three-phase.**

I. Introduction

MULTILEVEL inverters (MLIs) have been developed for more than five decades and gained increasing importance in industrial applications as one of the most attractive solutions for implementing medium-/high-voltage (HV) high-power converters [1]–[13]. The MLIs are configured by a distinct arrangement of single/several dc sources, namely batteries, rectifiers, flying capacitors (FCs), fuel cells (FUCs), photovoltaic (PV) panels, and semiconductor devices, e.g., insulated-gate bipolar transistor, metal–oxide–semiconductor field-effect transistor, and diodes, in a way to produce a near sinusoid voltage with low distortion. Combining low-voltage (LV) dc sources with semiconductors switches can efficiently generate HV stepped waveforms at the output of converters. The rating of the switches is defined by the rating of linked dc sources, so the voltage stress on the switches is much lower than the output voltage. From the 1970s, Baker and Bannister in [14] have invented the first converter topology, which is widely known as cascaded H-bridge (CHB) MLI, using several dc sources. Each source was linked to a single-phase inverter to form one cell. By connecting more cells in cascade as shown in Fig. 1(a), a multilevel output can be achieved. A few years later, in the 1980s, a single source multilevel topology called diode clamped or neutral point clamped (NPC) MLI has been proposed by Baker in [15]. Despite using one dc source, it requires several diodes that are connected to a neutral point, as shown in Fig. 1(b). In 1981, Nabae *et al.* [16] have presented the NPC implementation by using the pulsewidth modulation (PWM) scheme. Fig. 1(c) shows a FC or capacitor-clamped MLI, being introduced during the 1990s in [17] and [18]. Although it needs only one dc source, several FCs result in increasing both size and control complexity of the FC-MLI. These three topologies have considered as the basic MLI topologies in the literature [1]–[4]. The dc-to-ac conversions using MLIs are widely used in power systems, transportation, and renewable energy systems, for example, in flexible ac transmission systems [19], [20], high-voltage direct-current (HVdc) [21], [22], active power filters [23], [24], variable frequency drives [25]–[27], pumped storage power

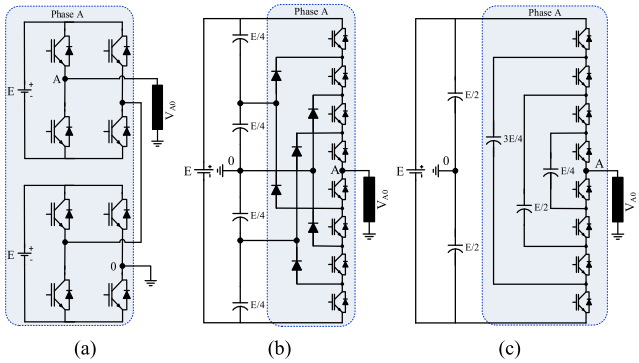


Fig. 1 One leg of the basic MLI topologies for five-level configurations. (a) CHB MLI. (b) NPC MLI. (c) FC MLI.

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plants [28]–[30] and grid-connected or standalone PV systems [31]–[33].

The MLI based dc to ac converters have several attractive merits as reported in [1]–[13]:

1) producing high-quality waveforms with low harmonic contents and low dv/dt stress, significantly reducing the total harmonic distortion (THD), filter dimensions, and electromagnetic interference (EMI);
2) operating in both fundamental and low frequency switching schemes can lower switching losses, being beneficial for efficiency and cooling requirement, especially in high-power applications;
3) using low-rated standard semiconductor devices for producing high voltage without connecting them in a series manner as in two-level medium-power inverters; and
4) having small/zero common-mode voltage (CMV) can eliminate drawbacks of CMV in many applications, for example, the stress in the bearing of a driven motor fed by MLIs can be reduced in drive systems.

Moreover, several MLIs have further strategic merits, namely transformerless operation, modularity, voltage, and current scalability, high redundancy in switching states, and fault-tolerant operation. On the other hand, these merits come with the cost of a high number of passive and active components, such as dc sources, FCs, inductors, diodes, and switches. Consequently, the volume, cost, and complexity of the inverter are increased [1]–[13]. Thus, proposing new MLIs, that can enlarge the level number along with a low component count is currently one of the key research trends in this research theme [3], [11]. Within the theme, improving efficiency, power density, control simplicity, reliability, cost, and broadening MLIs applications have attracted a large number of publications every year. Accordingly, reviewing the most advanced knowledge in this research field periodically is always of importance to update the research baselines or the newest reflections, resulting in many review studies presented in [1]–[13]. Most of those studies give a detailed review of MLIs based on a specific application or inverter family, e.g., transportation [8], medium-voltage drives system [13], modular MLIs [5]–[9], HVdc applications [10], and renewable energy integration [3]. Moreover, the existing reviews have used two conventional factors, namely the level-number per switch ratio (LSR) or component per level factor (CLF), to assess the component counts among topologies [34], [35], which are not able to take component ratings or cost and stresses of component into consideration.

To address the problem of existing comparative factors, this article proposes a novel comparative factor, so-called "component for each level (CEL)," in addition to a review of the most promising MLI topologies. Unlike the existing reviews focusing on a specific application, this article reviews diverse MLI topologies in a wide range of applications. Further, a comparative study is presented to verify that the proposed factor allows comparing the component count among MLIs more efficiently.

The rest of this article is organized as follows. Recently proposed voltage source MLIs will be classified and reviewed in Section II in detail, while both existing and the proposed methods for comparing MLIs will be discussed in Section III. Finally, the conclusion is drawn in Section IV.

II. Classification of MLIs

The recently developed MLI topologies are subdivided into three main groups based on the number of phases, i.e., single-phase, three-phase, and over-three-phase configurations as shown in Fig. 2. The selected topologies are allocated in different subgroups, namely single dc source, Multiple dc sources symmetrical MLIs, asymmetrical MLIs, transformer-based, and transformerless MLIs. The first two main groups are the main focus of this paper, being detailed in the following sections.

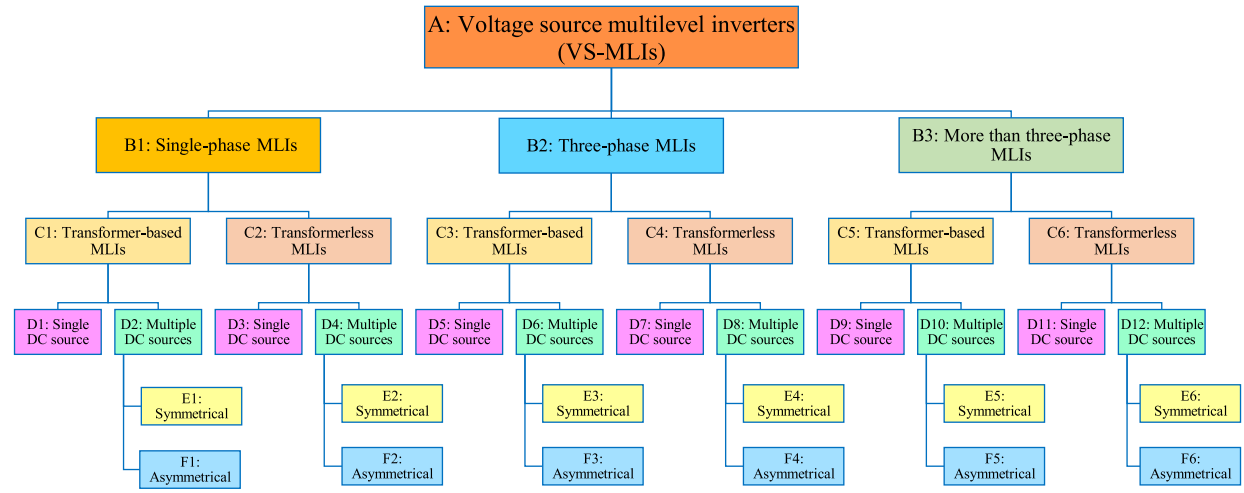
A. Single-Phase MLIs

This section presents a detailed review of the recently developed single-phase MLI topologies (or groups C2 and C1 in Fig. 2) in terms of construction, features and limitations. The addressed topologies are applied in renewable energy, motor drives, and power systems with diverse designs and characteristics. This review focuses on the MLI with a boosting capability, coupled inductors-based MLI, transformers-based MLI, specially designed topologies for particular applications and hybrid unipolar MLI topologies.

A novel single-phase MLI with the boosting capability is proposed in [36] as shown in Fig. 3, consisting of three stages, conventional boost converter, switch-diode-capacitor cell, and full H-bridge inverter. These three stages function as a step-up, level generator, and inversion stages, respectively. It can produce five voltage levels by using a single dc source, three power diodes, two capacitors, six switches, and an input inductor. Unlike other five-level inverters, the topology's main features include boosting capability, using a single dc source and low switch count. However, bulky size, high losses, and limited lifetime are still a problem since it requires capacitors, inductor, and a significant number of diodes. This circuit is suitable only for LV applications because of HV stress across the switches of the used H-bridge. To overcome these limitations, a quasi-CHB configuration was proposed in [37] as illustrated in Fig. 4(a), consisting of two cascaded modules for generating five levels. Each module has one dc source, one inductor, one capacitor, two diodes, and four power switches. The problem of limited generated voltage was solved by using modules in a cascaded configuration. To improve the performance of the topology under unbalances of the dc sources, resulting in a voltage difference in the existing capacitors, and a dc offset at output, an additional capacitor C_{d} has to be used between modules, as shown in Fig. 4(b). Although this capacitor has a LV rating, it must carry the entire load current.

Other C2-group MLIs based on coupled inductors have been presented in [38]–[40]. In [38], a π-type MLI was proposed for single-phase applications. Additionally, the upgrading possibility for three-phase applications was discussed in [39]. The π-type MLI consists of two three-terminal switch network (SN) as illustrated in Fig. 5(a), each SN is configured by using two switches and two diodes. The five-level circuit uses two dc sources, two capacitors, four diodes, and two coupled inductors. The coupled inductors are connected in series, and the connection point produces the output node A, while the outer terminals B and C are connected to the middle points of SNs. One of the key advantages of the presented topology is using only four switches

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A: In [36-83, 85, 86, 92-97, 101-104, 107, 109-116, 141-165]	C1: In [43, 46-54]	C6: In [143, 155, 160-165]	D4: In [36-42, 44, 45, 55, 56, 58-83, 85, 86, 102, 141-143]	D8: In [39, 95, 101-103, 109-115, 142, 143, 149, 152, 154-156]	E2: In [37-40, 42, 60-63, 65-67, 71, 78, 80, 82, 86, 102, 142]	F1: In [48, 50, 51]	F6: In [143, 162, 165]	
B1: In [36-83, 85, 86, 102, 141-143]	C2: In [36-42, 44, 45, 55-83, 85, 86, 102, 141-143]	D1: In [43-47, 49, 51, 53, 54]	D5: In [44, 45, 144-146, 159]	D11: In [155, 161, 164]	E3: In [51, 147, 148]	F2: In [58, 60-62, 64-66, 68, 69, 74, 76, 78-80, 82, 102, 143]		
B2: In [39, 44, 45, 92-97, 101-104, 107, 109-116, 141-159]	C3: In [44, 45, 144-149, 159]	D2: In [48, 50-52]	D6: In [147-149]	D12: In [143, 160-163, 165]	E4: In [39, 60, 78, 95, 101-103, 109, 110, 113, 115, 142, 154, 155]	F3: In [51, 149]		
B3: In [143, 155, 160-165]	C4: In [39, 92-97, 101-104, 107, 109-116, 141-143, 149-158]	D3: In [36, 39, 41, 42, 44, 45, 55-57, 59, 66, 70, 72, 73, 75, 77, 81, 83, 85, 86, 141]	D7: In [92-94, 96, 97, 104, 107, 116, 141, 150-153, 157, 158]	E1: In [51, 52]	E6: In [160, 161, 163]	F4: In [60, 78, 102, 109-112, 114, 143, 149, 156]		

Fig. 2 Classification of multilevel voltage source inverters.

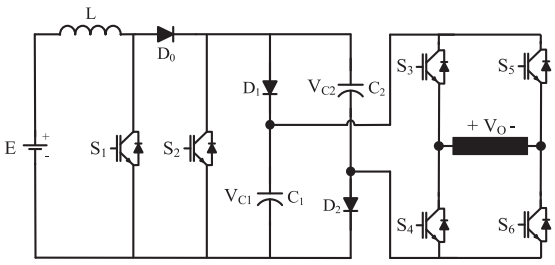


Fig. 3. Enhanced single-phase step-up five-level inverter [36]. Capacitor's voltage (V_{C1}, V_{C2}) = E/(1 - D_{S1}), where D_{S1} is the duty cycle of S_1.

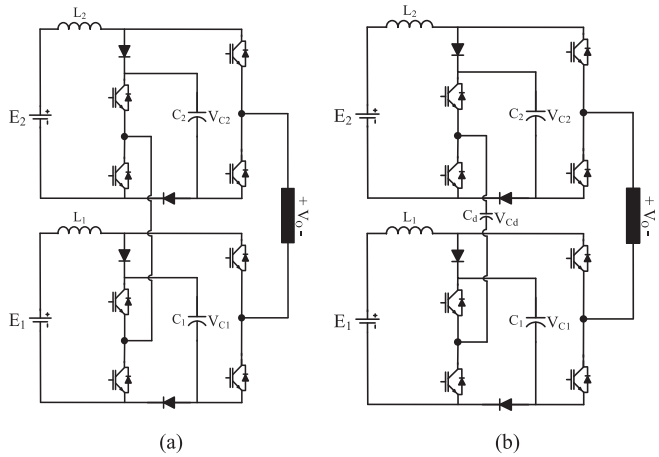


Fig. 4. Quasi CHB five-level boost inverter [37]. $V_{C1} = E_1/(1 - 2D_1)$, $V_{C2} = E_2/(1 - 2D_2)$, and $V_{Cd} = (D_1 - D_2)\,V_{(C1\ or\ C2)}$, where D_1 and D_2 are the shoot-through duty cycles.

for producing five voltage levels $+E/2$, $+E/4$, 0, $-E/4$, and $-E/2$ without using any FC, resulting in control simplicity with a moderate size. However, lack of modularity and using coupled inductors limit the applicability of the proposed circuit. Belong to the same family, four nine-level coupled inductors-based topologies were proposed and analyzed in [40]. Fig. 5(b)–(e) shows the suggested circuits, being formed by using two dc sources, switches, and pairs of coupled inductors. They have the common limitations of topologies in [38] and [39], but do not use any diode or capacitor.

Two-hybrid MLI topologies were proposed in [41] and [42], being formed by connecting three-level FC-fed-H-bridge (FCHB) cell with either three-level T-type cell in [41] or three-level active neutral-point-clamped (ANPC) cell in [42]. Connecting the FCHB cell with T-type or ANPC cells generates only five voltage levels of $-E/2$, $-E/4$, 0, $E/4$, and $E/2$, with a peak value equal to half of the dc-link voltage (i.e. 0.5E). Consequently, a two low-frequency switches (LFS) cell was recommended in [41] and [42] to increase the peak value and level count of the output voltage. The peak value becomes E (i.e., the full dc-link voltage), and the level count is enlarged to nine levels instead of five (the additional four levels are: $\pm E$ and $\pm 3E/4$). Fig. 6 shows the nine-level configurations of the presented topologies in [41] and [42]. Fig. 6(a) illustrates the presented topology in [41], consisting of three capacitors, ten switches, and one dc source, while the introduced topology in [42] requires twelve switches, three capacitors and one dc source for producing nine voltage levels, as depicted in Fig. 6(b). The two topologies have the same count and rating of the capacitors (two of $E/2$ and one of $E/4$), the switches in the LFS (two of E),

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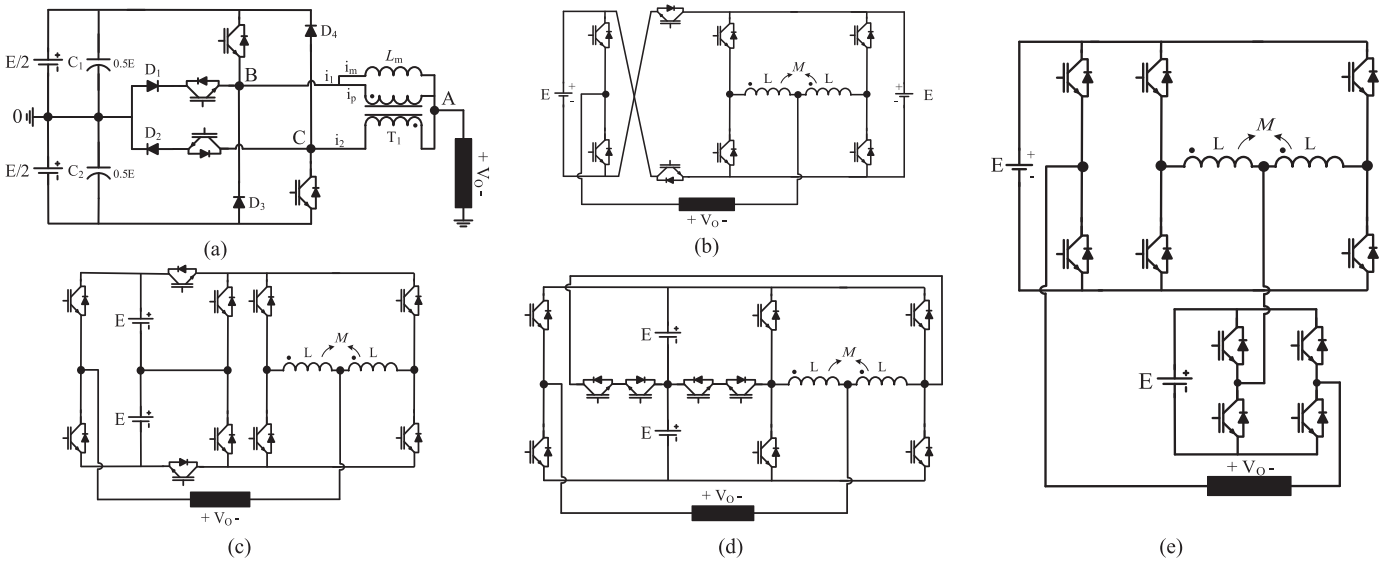


Fig. 5. Multilevel single-phase inverters with a pair of coupled inductors [38]–[40]. (a) Single-phase π-type five-level inverter [38], [39]. (b) Active series voltage sources with coupled inductors [40]. (c) Active NPC with coupled inductors (ANPC-CI) [40]. (d) Extended ANPC-CIs (EANPC-CIs) [40]. (e) Cascaded with coupled inductors (C-CIs) MLI [40].

and FCHB (four of *E*/4) cells, but they require different switch counts and ratings of the utilized switches in ANPC and T-type cells. The presented topology in [42] needs two more switches as compared to the topology in [41]. Although the switches of ANPC and T-type cells have the same total standing voltage (TSV) of 3*E*, they have different voltage ratings. All switches in the ANPC cell have the same voltage rating of *E*/2, while the switches in the T-type cell have different voltage ratings (two of *E* and two of *E*/2). From the industrial point of view, using switches of equal ratings is better than having different ratings, in terms of maintenance, manufacturing, and loss/temperature distribution, making the presented topology in [42] more advantageous than the presented topology in [41]. It is worth mentioning that the level count can be enlarged for both topologies by connecting additional FCHB cells. In [42], two methods were suggested (can be applied for the topology in [41] as well): either keeping a single dc source while repeating the FCHB cell or cascading the structure in Fig. 6(a) (or Fig. 6(b) for the topology in [42]) to construct a multiple dc source configuration. The two extension methods can be used as depicted in Fig. 6(c) for gaining more benefits, depending on the availability of dc sources and the required output voltage. Using a single dc source and the possibility for generating a higher number of voltage levels by adding FCHB cells are the main features of these circuits, besides using a low component count. However, requiring a significant number of different rating capacitors for enlarging the voltage level count increases the inverter footprint and control complexity. Moreover, using the two-switch cell across the dc link makes these topologies more applicable in LV applications alone.

Theoretically, the modularity feature enables producing an infinity number of voltage levels with HV values by using low-rating semiconductors but requiring a higher number of components. In this direction, the cascaded transformer MLI (CTMLI) family (or C1 group in Fig. 2) has been proposed for eliminating the needs for numerous numbers of DC sources and floating capacitors while suffering the cost of required transformers [43]–[54]. Fig. 7(a) and (b) shows the conventional CTMLI, and a reduced component version was reported in [43]. The conventional topology uses four switches tied with a low-frequency transformer as a building cell, while the circuit in Fig. 7(b) merges two cells to save almost half of switches count. Modularity, employing a single dc source, capacitor- and diode-free are the main merits while using bulky low-frequency transformers is the main demerit.

In [55]–[68], several topologies (belong to group D3 and D4 in Fig. 2) have been proposed for producing multilevel voltages as shown in Figs. 8–10. All of them use two stages, one for generating unidirectional multilevel dc voltage and the other one for changing the polarity of the generated voltage from the first stage to multilevel ac voltages. This common technique for obtaining ac voltage makes the mentioned circuits suffered from HV stresses across the switches in the second stage, reducing the permissible operating voltage and limiting them to LV applications. For example, the topology in [55] uses a new switched-capacitor (SC) as the first stage while a normal full H-bridge acts as a polarity changer stage for obtaining nine levels. Fig. 8(a) shows this topology, having a reduced component count and the ability to avoid the voltage balance problem by the inherent self-voltage-balance feature. Therefore, the switching algorithms get simplified. Despite using one dc source, it requires two capacitors, two power diodes, and nine switches with different ratings for generating nine levels. By using a new quasi-resonant SC (QRSC) circuit instead of the existing SC in Fig. 8(a), a new QRSC MLI has been developed in [56]. It allows producing *N* voltage levels by increasing the number of the capacitors, but it has HV stress across the switches of the H-bridge, lowering the input dc source voltage. Further,

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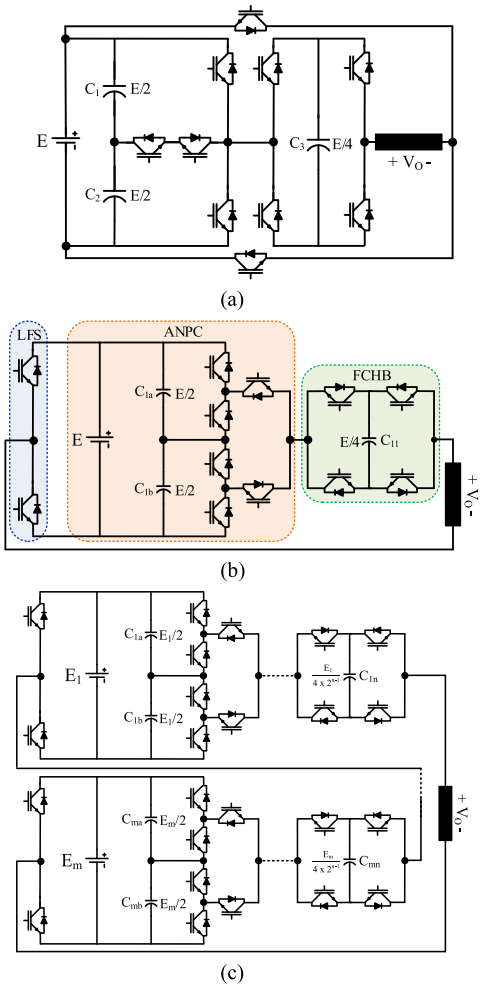


Fig. 6. Improved hybrid MLI topologies [41], [42]. (a) Nine-level inverter with reduced part count [41]. (b) Nine-level configuration of the double-hybrid ANPC inverter [42]. (c) *N*-level configuration for the double-hybrid ANPC inverter [42].

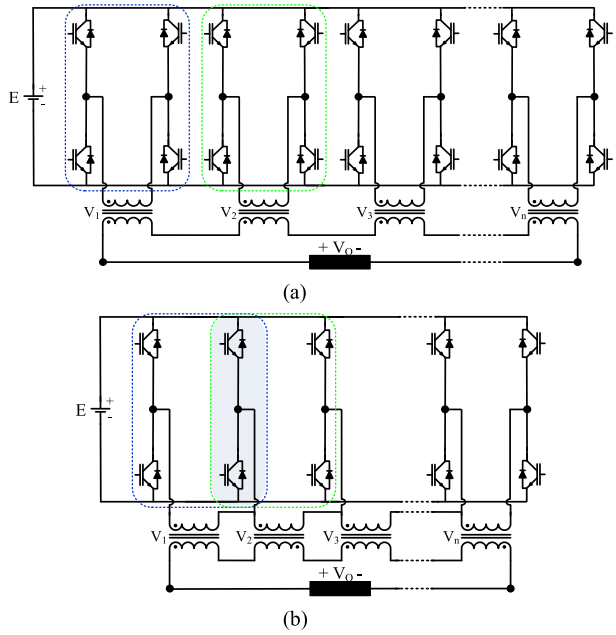


Fig. 7. Cascaded-transformer multilevel inverter [43]. (a) The conventional CTMLI. (b) Low component merged cells CTMLI in [43].

the self-voltage balancing feature can be realized by fully connecting the capacitors in parallel or partially to the load or source. Because of this connection, current spikes appear, increasing the capacitance, and decreasing the inverter lifetime. To overcome this challenge, the quasi-resonant inductor in the QRSC circuit is used to suppress these spikes, reducing the capacitance and prolonging the expected lifetime. Fig. 8(b) shows *N*-level version of QRSC topology, requiring one dc source, one inductor, *X* capacitors, *X* diodes, $2X+2$ switches, where $X = (N-1)/2$.

The proposed topology in [57] uses several unidirectional and bidirectional modules for building different substages, working as a level-generator (LG) stage. The H-bridge is to change the voltage polarity as demonstrated in Fig. 8(c), in which a single source inverter uses nine capacitors and 42 switches for producing 49 levels. Although the proposed circuit does not use any inductor, it can boost the low input voltage to a high value. The output voltage is limited only by the voltage rating of the H-bridge four switches. For example, the voltage stress across theses four switches will be $24E$ for $N = 49$ levels, where E is the input voltage. Boosting feature is obtained by charging several capacitors stage by stage in a cascaded manner, i.e., the capacitors of the current substage can be charged by the capacitors of the previous substages. Using a single low dc voltage source for producing high voltage levels is the main merit of this topology, in addition to the diode-, inductor-free features. However, using many capacitors (nine for the 49-level version) with different capacitances and voltage values makes the control schemes complicated, decreasing the reliability and lifetime of the converter. An improved topology based on this circuit has been published in [58], having almost the same structure for the first two stages except replacing the two capacitors by two dc sources. For the last stage, it uses several full H-bridge cells instead of only one in [57], avoiding using the single-phase H-bridge to change the voltage polarity or HV switches to obtain the negative voltage levels. Fig. 8(d) shows the complete configuration, producing 55 voltage levels by using seven capacitors, 44 switches and three asymmetrical dc sources.

Fig. 8(e) shows a new single-source seven-level topology investigated in [59], in which three-level dc-voltages are produced by using LG stages, consisting of a single dc source, three capacitors, four switches, and four diodes, Moreover, a traditional H-bridge was used for producing the negative part, being more suitable for LV applications alone. Using only one dc source is counted as an attractive advantage of this topology, but it has limitations regarding using diodes and capacitors as mentioned before. For example, to overcome the challenges for keeping the voltage of the capacitors in the dc-link balanced, the authors in [59] have recommended to use a resonant SC unit as highlighted in Fig. 8(e), increasing complexity, cost and the inverter size.

A new switched-capacitor MLI (SCMLI) was proposed in [60], which shares the same shortcomings like the topologies in [55]–[59] while using a new six-switch configuration for changing the polarity instead of using H-bridge. Further,

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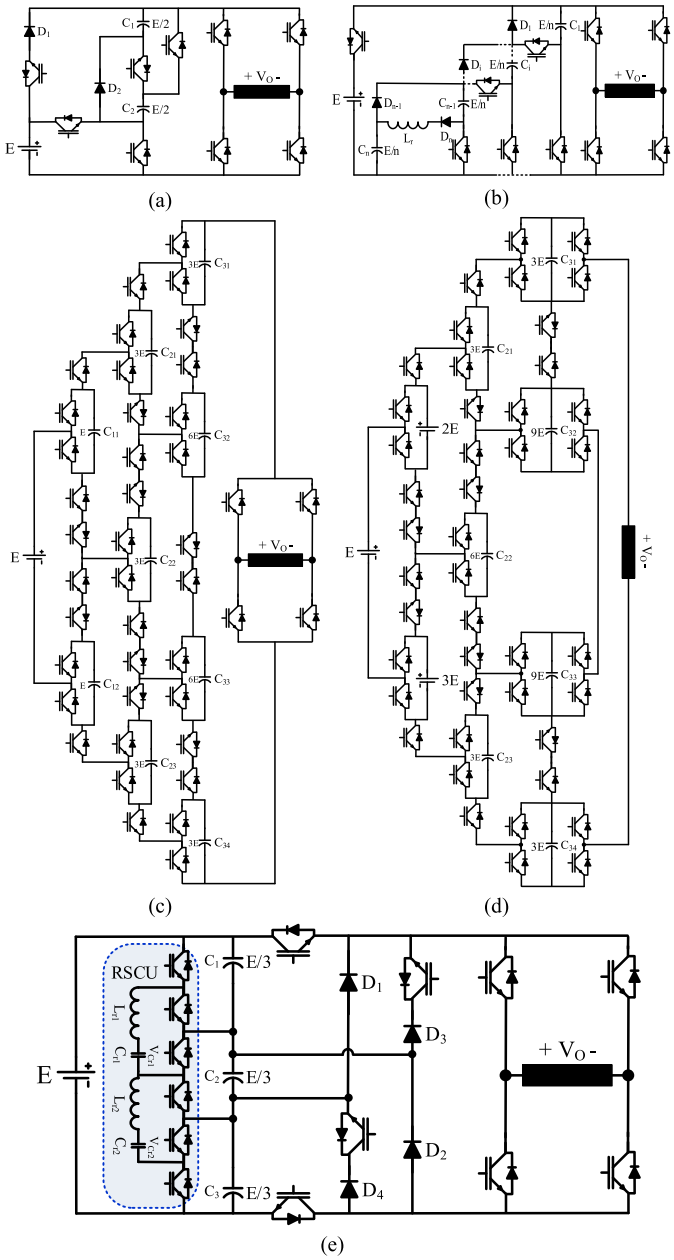


Fig. 8. Unipolar MLI topologies use polarity-changer stage for generating negative voltage levels [55]–[59]. (a) Nine-level inverter employing one dc source [55]. (b) Quasi-resonant switched-capacitor MLI [56]. (c) Step-up MLI with a single dc source [57]. (d) MLI structure based on a combination of SC and dc sources [58]. (e) Single source seven-level MLI topology [59].

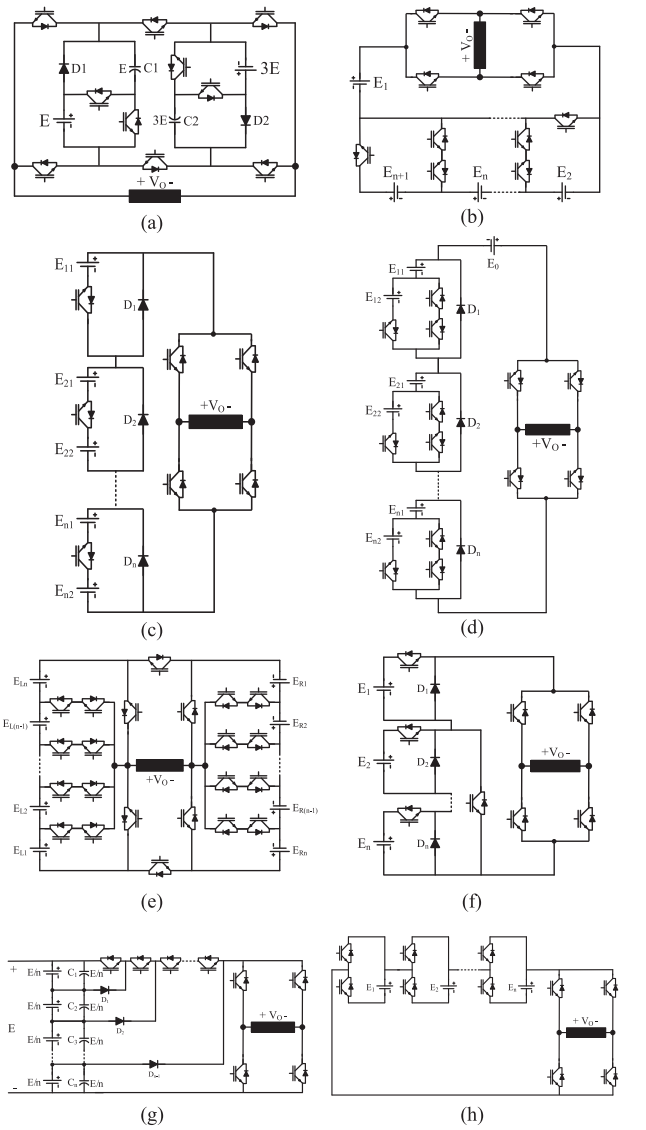


Fig. 9. Unipolar MLI topologies with the polarity-changer stage for generating negative voltage levels [60]–[67]. (a) 17-level structure for the single-phase SC-MLI [60]. (b) MLI for symmetric and asymmetric structures [61]. (c) MLI topology using single source and double source modules [62]. (d) Symmetric switched diode MLI [63]. (e) Cascaded switch-ladder MLI [64]. (f) Cascaded switched-diode MLI [65]. (g) Switched capacitor-diode MLI [66]. (h) Switched-battery boost-MLI [67].

multiple asymmetrical dc sources are used instead of using a single source, and voltage generator cells are required for generating multiple dc-link voltages. Each one consists of two switches, one capacitor, one diode, and dc source. A 17-level version of the proposed MLI is shown in Fig. 9(a), requiring ten switches, two capacitors, two diodes, and two isolated dc sources having asymmetrical values of E, and $3E$, respectively. To increase the output levels with a reduced component count, several topologies in the same family were proposed and summarized in Fig. 9(b)–(h), being detailed in [61]–[67]. As seen from Fig.9(b)–(h), their key characteristics are realized as diode-, capacitor- inductor-free, boosting capability, using only a single dc source, a high number of capacitors, inductors, and dc sources. However, they suffer from a common drawback, i.e. using polarity-changer stage, making the output voltage limited by the rated voltage of the switches.

A recently developed member of the unipolar MLIs family was proposed in [68]. Fig. 10(a) shows the nine-level asymmetric structure of this topology, consisting of a unipolar level generator part followed by a conventional H-bridge cell to obtain bipolar multilevel voltages, similar to the topologies in [55]–[67]. Fig. 10(a) shows the proposed topology, in which two trinary asymmetrical dc voltage sources (E_1:E_2 is 1:3) and ten switches are necessary for producing nine voltage levels of

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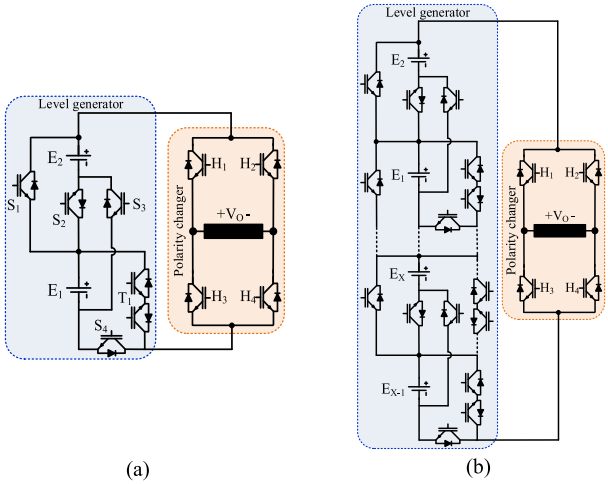


Fig. 10. Asymmetrical MLI with trinary sequence proposed in [68]. (a) Nine-level configuration. (b) Generalized configuration for producing 3^X-level by using X dc sources.

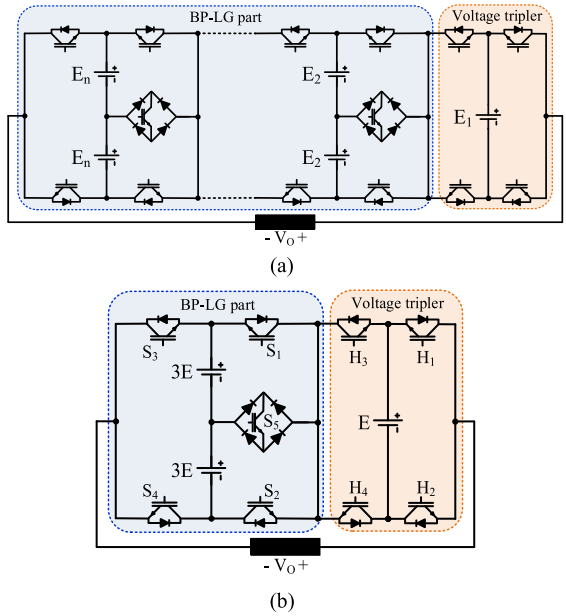


Fig. 11. Asymmetrical MLI topology proposed in [69]. (a) Generalized configuration. (b) Fifteen-level configuration.

4E, 3E, 2E, E, 0, $-E$, $-2E$, -3E, and -4E. As suggested by the authors in [68], the voltage level count can be enlarged to 3^X levels by adding ($4K$+2) switches and "X" dc sources, as depicted in Fig. 10(b). The proposed topology has remarkable merits, namely reduced component counts, and being capacitor-, and inductor-free. However, the high TSV of switches in both level generator and polarity changer parts is considered its main demerit. For example, the switches of the polarity changer H_1-H_4 must block the full dc-link voltage (i.e., $E_1+E_2+\ldots+E_X$), in addition to the different HV stress across the remaining switches based on their location in the level generator part. The TSV will be further increased when the level count or output voltage needs to be higher. The standing voltage is equal to $(((2(3^X-1)-3)+4(2(3^X-1)-3))E)$, where X is the number of dc sources. Accordingly, this topology is highly recommended for LV applications, where high voltage levels are required at a low maximum output voltage.

Unlike the MLIs in [61]–[67], that use the level generator stage to produce a unipolar multilevel voltage and a polarity changer to obtain bipolar multilevel voltages, resulting in high voltage stresses across the polarity changer switches, Majumdar *et al.* [69] used bipolar units and a full H-bridge cell to construct a novel asymmetrical MLI topology. Fig. 11(a) shows the generalized configuration of the proposed topology, in which the bipolar units act as a bipolar level generator (BP-LG) while the H-bridge is used to triple the voltage level count of the BP-LG part. For example, to produce fifteen levels, one five-level bipolar unit, which is linked to the H-bridge cell, is required as depicted in Fig. 11(b). The bipolar unit uses two equal dc sources of 3E, generating five levels of 6E, 3E, 0, -3E, and -6E, while the H-bridge uses single dc source of E to generate three levels of E, 0, and $-E$. Accordingly, fifteen voltage levels can be synthesized. The fifteen-level configuration of the proposed topology requires nine unidirectional switches and four power diodes. The main feature of this topology is its ability for producing HV level count while having structure modularity and using a low number of components and active switches. However, its disadvantages include requiring high counts of dc sources and power diodes when enlarging the voltage levels and the high voltage stresses across the switches of the bipolar unit. For example, in the fifteen-level configuration, S_1–S_4 have to block voltages of 6E, and S_5 must block 3E. When using a second bipolar cell to produce 75 levels, the voltage stresses become 30E and 15E for the corresponding switches in the second unit. It is worth mentioning that this topology can produce N level either by increasing the number of bipolar cells as in Fig. 11(a) or/and connecting several modules in cascade [each module has the same structure as the circuit in Fig. 11(b)]. More details for optimized selections of both cell and module counts can be found in [69].

A newer single source inverter was proposed in [70], consisting of H-bridge integrated with a bridge-modular-SC unit in a way to produce multilevel output with boosting capability. Fig. 12(a) shows the generalized configuration that uses SC blocks for increasing the voltage level. The boosting capability is a function of the SC blocks number (N_{sc}). The maximum output voltage V_o will be equal to $4*N_{sc}*E$. For example, using one SC block can produce five levels with the gain of four. Fig. 12(b) shows the five-level circuit, requiring twelve switches, four capacitors, and one dc source. The traditional CHB MLI uses only eight switches and two isolated dc sources for producing the same levels number with a lower output voltage about 50% (e.g. $E = 50$ V, $V_o = 100$ for CHB, and 200 V for the proposed topology). On the other hand, in the proposed topology, the voltage stress is a function of N_{SC} while in CHB, it is not related to the number of generated levels.

MLIs topologies with the predefined features for specific applications have been designed in [71]–[75]. Jain and Sonti [71] have proposed a new five-level configuration for minimising

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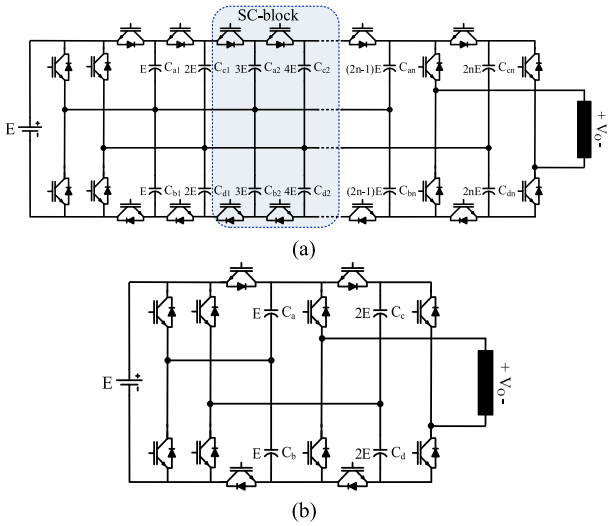


Fig. 12. Flying-capacitor-clamped MLI (FCC-MLI) [70]. (a) Generalised configuration. (b) Five-level configuration.

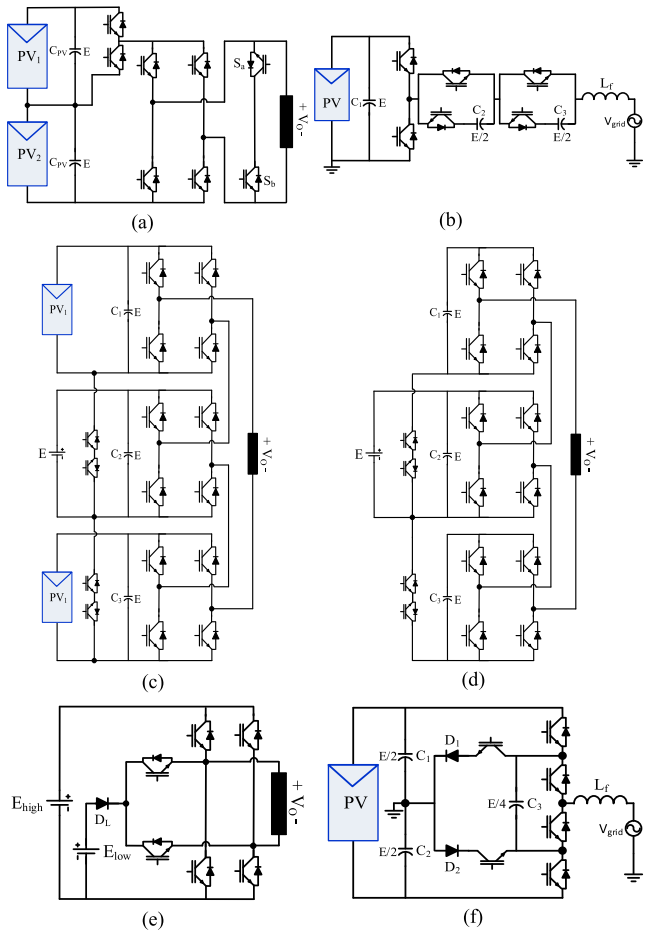


Fig. 13. MLI topologies have predefined features for specific applications [71]–[75]. (a) Five-level topology for PV systems [71]. (b) Transformerless MLI that eliminates leakage current in the PV system [72]. (c) Seven-level SC topology: when PVs are available during the day [73]. (d) Seven-level SC topology: when PVs are not available during the night [73]. (e) Dual-dc-port asymmetrical MLI [74]. (f) Six-switch five-level topology[75].

the leakage current in transformerless PV systems. Fig. 13(a) shows the proposed converter, consisting of two capacitors, eight switches, and two dc sources (to emulate two PV sources) for producing five levels. The basic concept here is to isolate the PVs from the grid during the zero-voltage state by turning OFF the four switches in H-bridge and using S_a and S_b for forming a new current path. Accordingly, the flow of the leakage current through the parasitic capacitance will be minimized. The switching losses in the switches of the H-bridge will be reduced effectively by enabling a complete turn-OFF for each half-cycle. On the other hand, the topology in [72] can eliminate the leakage current by connecting the negative terminal of PV to the grid neutral terminal. Therefore, the stray capacitance will be bypassed. Fig. 13(b) shows the five-level circuit for the proposed topology in [72]. As compared to the topology in [71], it can eliminate the leakage current in the PV system by using only six switches, three capacitors, and one dc source (to emulate PV source).

For a PV harvesting system, Sun *et al.*[73] have developed a new seven-level topology for PV-battery three-input converter applications, including three CHB, one dc source, three capacitors and two switches for charging purpose. The functionality of the proposed circuit can be explained by two operating modes: when the solar energy is available for PVs during the day, the inverter will be used as a three-CHB topology for producing seven levels, as shown in Fig. 13(c). While during the night when the PVs are OFF, the converter will operate according to Fig. 13(d), producing seven levels by using only one single source and three capacitors instead of three isolated dc sources (two sources emulate two PV generators) in the first mode.

In some situations, there is a need for connecting two renewable energy sources that generate a different voltage, e.g., PVs and FUCs to load/grid simultaneously by using fewer conversion stages to obtain high efficiency. To address this issue, dual-dc port MLIs (DP-MLIs) was developed in [74], presenting a new five-level DP-MLI. Fig. 13(e) shows its simplified version based on T-type inverter, consisting of two asymmetrical dc sources, one diode, six switches. As seen in Fig. 13(e), only one dc port is used for an HV source while the LV source is connected to the lower port. For grid-connected PV applications, the authors in [75] have developed six-switch 5L-ANPC based on the five-level active NPC inverter (5L-ANPC) as shown in Fig. 13(f). As named, it uses only six switches instead of eight switches like in the traditional 5L-ANPC for producing five levels while requiring two diodes. The idea of reducing the active switches count is based on the fact that for the grid-connected PV system, the grid voltage and output current are required to be in phase, so it is possible to ignore some paths for reactive current, i.e., some switches can be replaced with diodes.

A new member of the asymmetrical MLI family was proposed in [76]. This topology has a novel arrangement of components for generating high output levels by using a reduced component count module. Each module needs only 10 switches and four asymmetrical dc sources for producing 13 levels. Fig. 14 shows a 25-level configuration, consisting of two primary modules. Although switches have HV stress, especially S_3 and S_4, the

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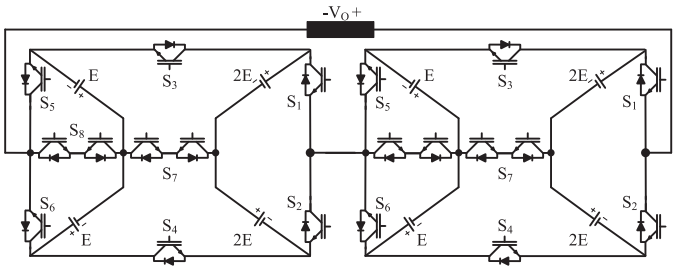


Fig. 14. Envelope type (E-Type) asymmetric MLI [76].

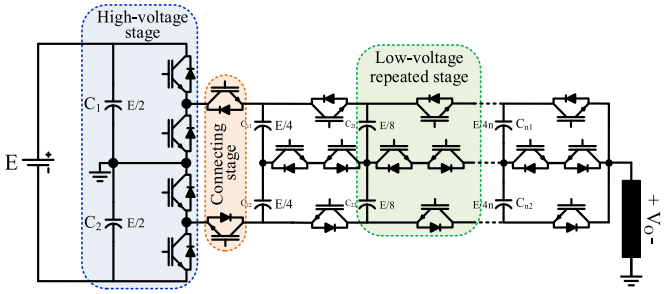


Fig. 15. Hybrid VSI based on T-type topology [77].

proposed circuit is more applicable in HV high-power industry because of its modularity feature. Inspired by its shape, it is called as envelope type MLI.

Hybrid MLIs have been an attractive trend in literature. Xu *et al.* [77] have presented a hybrid *N*-level topology using only one dc source. It has three stages: HV stage, connecting-switches stage, and LV stage, as seen in Fig. 15. The first and second stages are fixed while the third stage can be repeated for enlarging the voltage level number. Employing single dc source is one of the main advantages of this configuration while increasing the cost of having a high number of capacitors is a problem. For this reason, the authors have suggested using the second stage to create extra redundant switching states for making the voltage balance of the FCs easier. One repeated stage, e.g., T-type unit-along with the two fixed stages, is needed for producing five levels, requiring ten switches, four capacitors, and one dc source.

A cascaded MLI with a reduced component count was proposed in [78], in which each module has four asymmetrical dc sources. In addition to the four dc sources, it can produce 25 voltage levels with ten switches and eight diodes or can produce only nine-level if using symmetrical dc sources. Connecting modules in cascade results in the *N*-level configuration of the proposed MLI, as shown in Fig. 16. Each module has two "*E*" and two "5*E*" dc sources. The capability of producing negative and positive voltages without using the end-side H-bridge is considered one of the key merits of the proposed MLI. However, HV stress across the switches is the main limitation. For example, the right-hand switches S_1, S_2, S_3, and S_4 have voltage stresses of $2{*}5E$ while those stresses over the left-side switches S_5, S_6, S_7, and S_8 are $2{*}E$. Moreover, switches S_R and S_L have voltage stresses of $5E$ and E, respectively. The second asymmetrical *N*-level topology was presented in [79], being divided into fixed

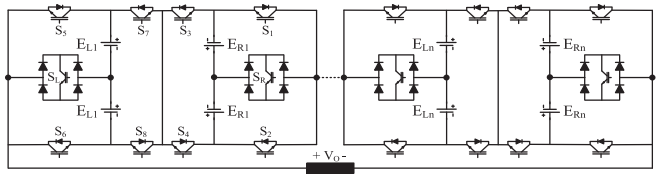


Fig. 16. Cascaded MLI based on a new module with symmetric or asymmetric dc sources [78].

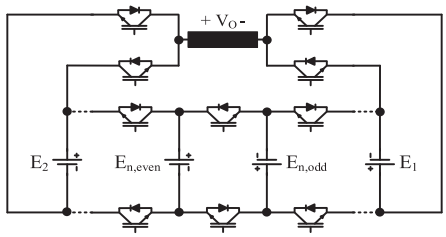


Fig. 17. Asymmetrical MLI with a reduced number of switches [79].

and repeated stages. The *N*-level configuration is shown in Fig. 17, in which the fixed stage consists of four switches and two dc sources while the repeated stage comprises two switches and one dc source. Although it uses many asymmetrical dc sources for increasing the levels number, it does not use diodes and capacitors, being more attractive features. For generating 15 levels, it requires only eight switches, and three dc sources with a magnitude of E, $2E$, and $5E$. It is worth mentioning that the voltage stress of the switches is a function of levels number. For example, producing 15-level requires four pairs of switches withstand for voltage stresses of $2E$, $7E$, E, and $4E$, fitting well for LV applications.

A group of cross-switched topologies was introduced in [80]–[82]. Connecting two T-type legs back-to-back was presented in [80], resulting in a new cross-switched T-type based MLI. It uses two cross-connected switches to connect two identical T-type modules in a back-to-back manner, as illustrated in Fig. 18(a). The cross-switched T-type MLI requires six unidirectional switches (S_1-S_6), two bidirectional switches (T_1 and T_2), and four dc voltage sources (E_1-E_4) to produce nine voltage levels of -4*E*, -3*E*, $-2E$, $-E$, 0, *E*, 2*E*, 3*E*, and 4*E* when using symmetrical dc sources ($E_1 = E_2 = E_3 = E_4 = E$), while seventeen voltage levels can be synthesized for the asymmetric operation ($E_1 = E_2 = E$, and $E_3 = E_4 = 3E$). The high voltage stress across the six unidirectional switches is considered as the main disadvantage of this topology. For example, in the symmetrical operation, the voltage stress across switches S_1-S_4 is $2E$, while it is equal to $4E$ for both S_5 and S_6. The situation becomes worse for the asymmetrical mode of operation, where the voltage stress is $2E$, $6E$, and $8E$ for switches (S_1 and S_2), (S_3 and S_4), and (S_5 and S_6), respectively. Low component count, being capacitor-, inductor free, and generating negative voltage levels without using H-bridge are its advantageous features. Another merit of this circuit is the extension possibility. The level count can be enlarged to *N* levels by cascading the configuration in Fig. 18(a), as recommended by the authors in [80] and shown in Fig. 18(b).

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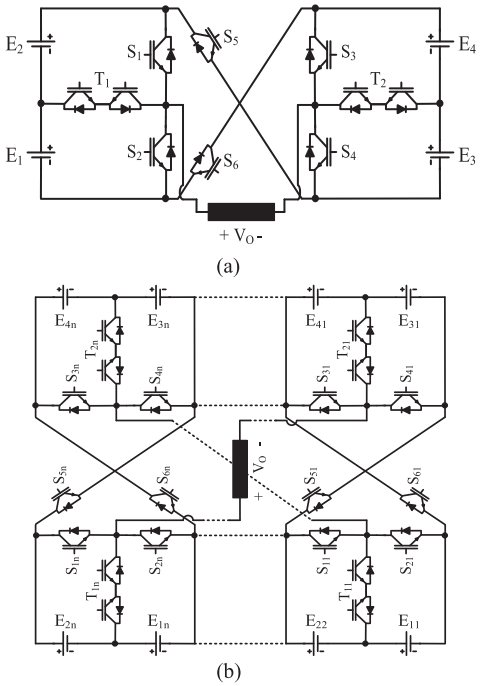


Fig. 18. Cross-switched T-type MLI [80]. (a) Nine-, seventeen-level configuration. (b) Generalized configuration.

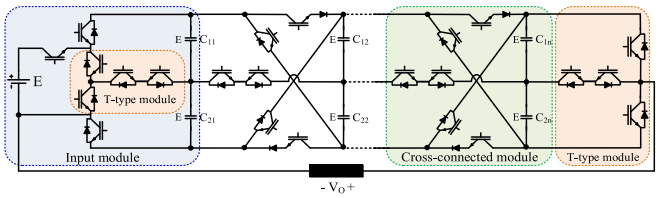


Fig. 19. Generalized configuration of the step-up topology in [81].

For producing N levels, $(1.25N-1.25)$ switches and $(0.5N-0.5)$ dc sources are required for the symmetrical operation, while under the asymmetrical mode, these numbers become $5(N-1)/8$ switches and $(0.25N-0.25)$ dc sources.

Unlike the cross-switched topology in [80], where only T-type modules are integrated with two cross-connected switches, Khenar *et al.* [81] use the T-type module accompanied with two new modules for forming a single-source step-up MLI topology. Fig. 19 shows its generalized configuration, consisting of three structures: T-type module, cross-connected module, and input module. Among these three modules, only the cross-connected module can be repeated to configure an extendable structure. The N-level voltage requires $(N-1)/2$ capacitors, $((1.5N-1.5)+5)$ switches, and $(0.5N-2.5)$ diodes. For example, for building a thirteen-level configuration, six capacitors, twenty-three switches, and four diodes are required in addition to one dc source. The proposed topology can step up the input voltage (E) to reach a required value by using several capacitors, acting as floating power supplies. Each capacitor is charged to E, boosting the input voltage by a gain of $(N-1)/2$. However, this feature results in a problem of increasing the number of

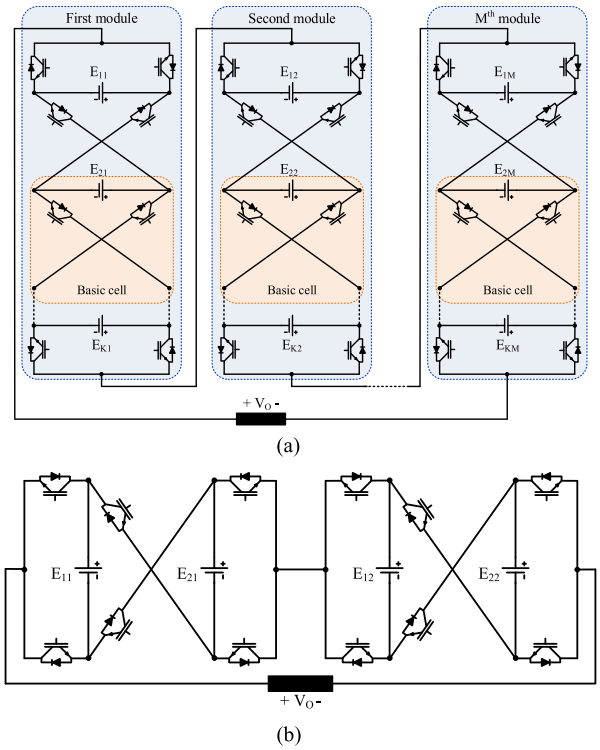


Fig. 20. Cascaded cross-switched topology in [82]. (a) Generalized configuration. (b) Nine-, 49-level configuration.

capacitors, or size, and control complexity. Further, the current spikes, that are common in several switched capacitor topologies [81], need to be reduced by some strategies as detailed in [81]. On the other side, the proposed topology has some of the remarkable merits, such as producing higher counts of voltage level without increasing the voltage rating of switches (voltage stress does not exceed $4E$) and generating bipolar voltage waveforms without the need of an H-bridge.

Another member of the cross-switched MLIs was presented in [82]. It is a cascaded cross-switched topology that can be configured with symmetric or asymmetric dc sources for producing a high-resolution output voltage. Fig. 20(a) shows its N-level configuration, consisting of cascaded M modules. Each module is structured by using K basic cells in cascade. The output level count can be enlarged by increasing the number of either module or basic cells, or both of them. For example, $(2MK+1)$ and $(4K-1)^{\mathrm{M}}$ voltage levels can be obtained from symmetrical and asymmetrical dc sources, respectively, if using (MK) dc sources and $(2MK+2M)$ switches. Kangarlu *et al.*[82] recommended a configuration, as shown in Fig. 20(b), being constructed by using two modules, where each has two basic cells (i.e. $M = 2$ and $K = 2$). It requires twelve switches and four dc sources for producing nine and 49 levels for symmetrical and asymmetrical operations, respectively. Besides features of being capacitor- and inductor free, the modularity is considered its main merit, allowing for producing N-levels without increasing the TSV of the switches. Having a low standing voltage of switches requires many isolated dc sources, making this topology more applicable to PV systems.

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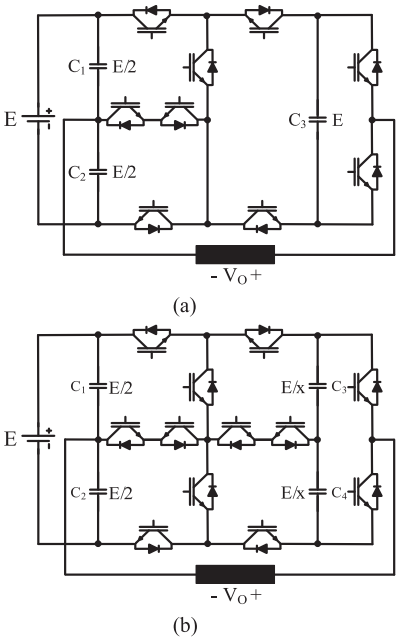


Fig. 21. Boost ANPC-MLI proposed in [83]. (a) Structure A, seven-level boost ANPC. (b) Structure B, nine-level (X= 4) or eleven-level (X= 1) boost ANPC.

A boost active-neutral-point-clamped MLI (ANPC-MLI) was recently proposed in [83], which was derived from an improved five-level ANPC topology in [84]. As compared to the topology in [84], the topology in [83] improves both the voltage gain and level count. The voltage gain can be improved from 1 to either 1.5 or 2.5 while the level count is increased to seven, nine, and eleven levels. These positive features must be compensated by an increase of the switch and FC counts. Fig. 21 shows both structures of the proposed topology in [83], in which the structure A can generate seven voltage levels with a voltage gain of 1.5, requiring only one extra switch as compared to the five-level ANPC topology in [84]. The structure B can produce nine and eleven voltage levels with the voltage gains of unity and 2.5, respectively, increasing one FC and three switches as compared to the topology in [84]. The level count in the structure B has two values (nine or eleven) based on the charged voltage of the two FCs C_3 and C_4. When being charged to 0.25E, the obtained level count is nine. The level count becomes eleven when being charged to E. It is worth mentioning that the voltage stress across switches cannot exceed E for generating seven and nine voltage levels. The voltage stress does not exceed 2E for producing eleven voltage levels.

To combine the merits of quasi-Z-source (qZS) and MLIs, the concept of qZS was applied to MLI topologies [85]–[87], resulting in a family of buck-boost single-stage MLIs with the shoot-through withstanding capability. Husev *et al.* [85] proposed a new qZS multilevel topology based on the diode-clamped five-level inverter as depicted in Fig. 22. Two identical qZS networks are used for boosting the input voltage of a single dc source by a factor of B_f, where B_f is equal to E'/E_{in} and called boost factor. Then the five voltage levels of $-B_f E$, $-0.5B_f E$, 0, $0.5B_f E$, and $B_f E$ are generated by the diode-clamped structure. Fig. 22 shows

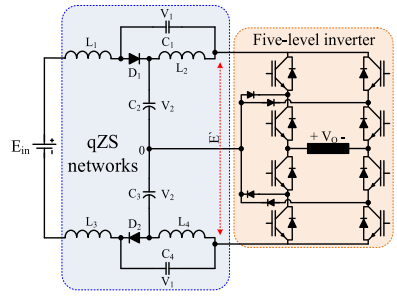


Fig. 22. Five-level qZS inverter proposed in [85]. $V_1 = DE_{\text{in}}/(2 - 4D)$, $V_2 = (E_{\text{in}}(1 - D))/(2 - 4D)$, where D is the shoot-through duty cycle.

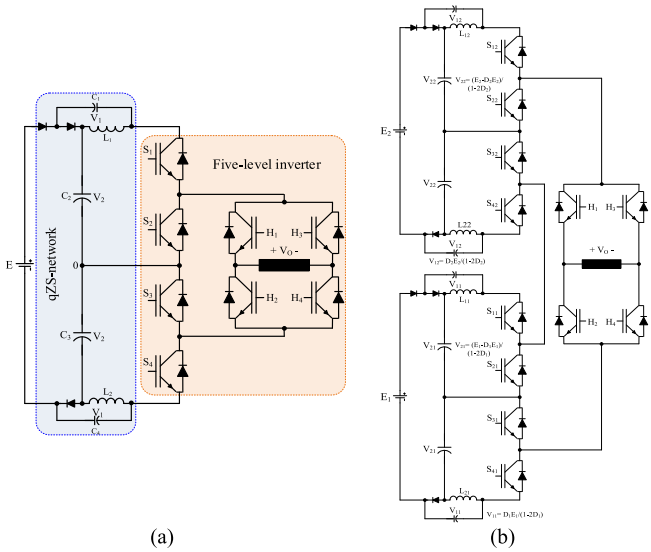


Fig. 23. Modified qZS MLI in [86]. $V_1 = DE/(1 - 2D)$, $V_2 = (E - DE)/(1 - 2D)$, where D is the shoot-through duty cycle. (a) Five-level configuration. (b) Nine-level configuration.

the proposed circuit, producing five voltage levels when using eight switches, six diodes, four inductors, four capacitors, and a single dc source. It is noted that the presented configuration in Fig. 22 can be extended to a three-level three-phase qZS inverter by adding one more inverter leg (four switches and two diodes) [85]. Using low-rated switches, single dc source, and continuous input current are the advantageous features of the proposed topology. On the other hand, increasing the number of diodes in the circuit and having a boost factor similar to the classic qZS inverter are considered as its main shortcomings [86]. A novel qZS topology was proposed in [86], integrating a modified impedance network with the MLI topology introduced in [88]. Fig. 23(a) shows its five-level configuration, in which four capacitors, two inductors, and three diodes are used for constructing the modified impedance network while six switches are used for producing multilevel output. The proposed topology requires a lower component count as compared to the five-level qZS-MLIs in [85] and [87], reducing the inductor count by 50% while keeping the same count of switches and capacitors. As compared to the topology in [87], it saves one dc source, but requires one extra diode. When comparing

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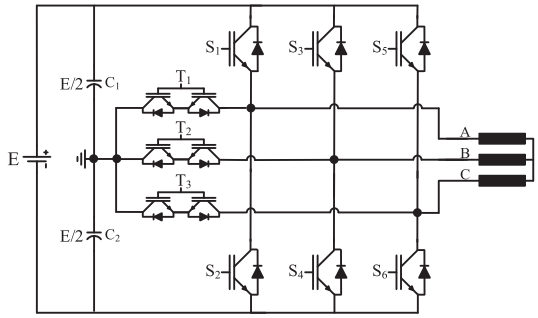


Fig. 24. Three-phase T-type MLI [92]–[94].

with the circuit in [85], it reduces the diode count by three diodes.

Further, the proposed topology can double the boost factor, which is not possible in [85] and [87]. To achieve these remarkable features, the current stresses of inductors (L_1 and L_2) and the voltage stresses of four switches (H_1-H_4) are doubled. It is worth mentioning that the switches H_1-H_4 are necessary for producing bipolar voltage waveforms and have a rating of full dc-link voltage. Their voltage stress also rises when enlarging the level count. For example, Fig. 23(b) shows the nine-level configuration of the proposed topology, in which two five-configurations are cascaded, doubling the voltage stresses across switches the H_1-H_4.

B. Three-Phase MLIs

This section presents a review of the recently proposed three-phase MLIs based on their operation, advantages, and disadvantages, making the selection of suitable applications easier. The reported topologies in this section represent different types of MLIs, such as single source, inductor-based, symmetrical, asymmetrical MLIs for hybrid, and nonhybrid configurations. Further some topologies for improving the power quality of power system are included.

One of the salient members in the neutral-point clamped MLIs family is the T-type inverter. It is also known as a neutral-point-piloted inverter and considered as one of the most popular three-level topologies [89], [90]. A single-phase T-type inverter was patented by Conergy in [91], and Schweizer *et al.* [92] presented the three-phase T-type configuration. Fig. 24 shows the T-type inverter for three-phase applications, consisting of a conventional two-level voltage source inverter (2L-VSI) combined with three branches of bidirectional switches, being assumed as a common-emitter configuration. Each branch connects the midpoint of the dc link to one leg of the two-level VSI, forming a T-type shape. The six switches of the VSI (S_1-S_6) are rated at the input voltage E, while the remaining switches have voltage ratings of $0.5E$. One counterpart to the T-type MLI is the diode-clamped MLI, which requires six clamping diodes while the T-type uses six switches instead. Both of them uses a single dc source and 2 capacitors, and 12 switches for producing three voltage levels. The distinct feature of the diode-clamped inverter is that it has lower voltage stresses of the switches ($0.5E$) than those in the T-type (six switches of E, six switches of $0.5E$), reducing the switching losses. On the other hand, the T-type inverter has a lower component count in the current path, reducing the conduction losses. Further, only one switch is required in the current path for positive or negative output voltage while two switches are needed in the diode-clamped inverter regardless of the output level [90]–[94]. Accordingly, the T-type MLI is more advantageous in applications, requiring low switching frequencies alone.

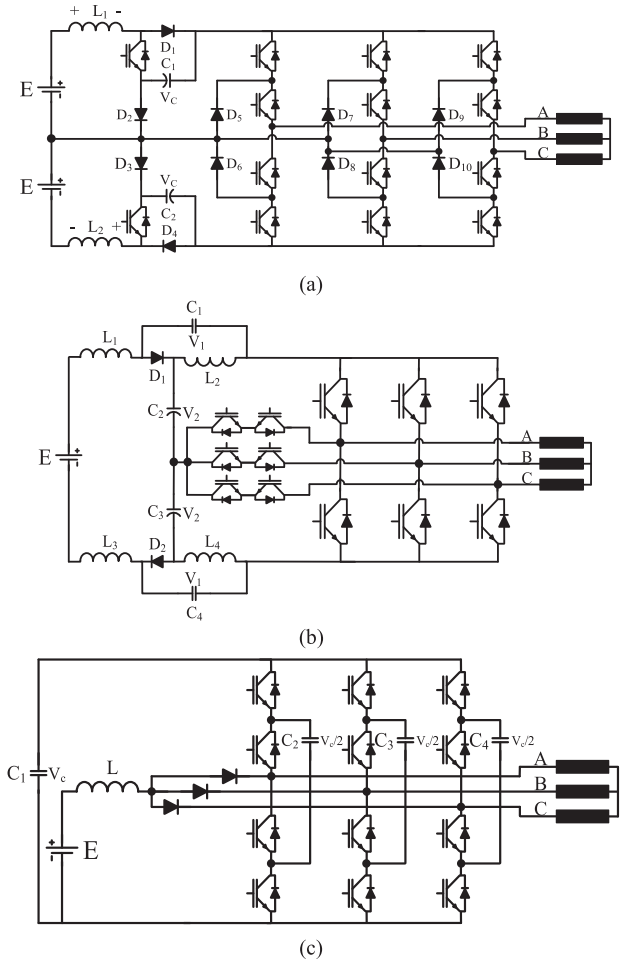


Fig. 25. Single-stage MLIs with boosting capability [95]–[97]. (a) Three-level LC-switching-based voltage boost NPC MLI [95]. $V_c = E/(1 - 2D)$, where D is the shoot-through duty cycle. (b) qZS inverter with a T-type MLI [96]. $V_1 = DE/(2 - 4D)$, $V_2 = (E(1 - D))/(2 - 4D)$, where D is the shoot-through duty cycle. (c) Three-phase three-level FCs split-source MLI [97]. To maintain a three-level operation, V_C should be larger than $2E$.

Single-stage MLIs (SS-MLIs) with boosting capability have been recently proposed in [95]–[97] for PV, uninterruptible power supplies (UPS), and FUCs applications. Typically, the boosting stage and multilevel stage are merged to form single-stage converters that have both merits of boost converters and MLIs. For example, a new SS-MLI called three-level LC-switching based NPC, was presented in [95]. Fig. 25(a) shows its complete configuration, consisting of a boosting circuit (BC) connected to a conventional three-level NPC, allowing for the capability for boosting the input voltage and producing improved

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quality output. The BC consists of four diodes, two switches, two inductors, and two capacitors, while twelve switches, six diodes, and two dc sources are required for the three-level NPC circuit. Compared to the conventional Z-source MLIs in [98] and [99], the proposed topology reduces 50% of capacitor and inductor count, and having a continues input current, but uses two extra diodes and two switches. In addition to the NPC limitations, using several high-power passive elements in the boosting stage increases the weight, cost, complexity, and the losses of the inverter.

Another topology of SS-MLIs with the boosting feature was introduced in [96], producing the same voltage levels like the topology in [95]. Instead of using NPC, the topology in [94] uses a T-type MLI to produce multilevel waveforms. Two identical qZS networks are used for the BC, as shown in Fig. 25(b). Compared to the topology in Fig. 25(a), only two diodes are required by using the T-type MLI. Without using switches in the BC, the count of capacitors and inductors is doubled. Three bidirectional switches in the topology increase the redundancy of the switching states, enabling fault-tolerant capabilities for some common faults, e.g., open-circuit failures. Fig. 25(c) shows a new three-level topology proposed in [97], having the same number of the levels in [95] and [96]. This topology is an upgraded configuration of the two-level split-source inverter in [100]. Because of its ability for generating a boosted voltage with three-level waveforms, the direct connection of LV energy sources, namely PVs and FUCs, become more accessible and efficient. Producing three levels needs twelve switches, three diodes, four capacitors, one inductor, and one dc source. The proposed topology has several attractive features, such as boosting capability, using a single dc source, continuous input current, and having a reasonable number of passive components. On the other hand, several limitations can be found as high-current and -voltage stresses on the used semiconductor devices, lack of modularity, increasing the control complexity and system footprint, decreasing the expected lifetime because of using FCs and inductor. Further, this topology needs extra efforts in control algorithms for removing the low-frequency components from not only output voltages but also input currents caused by voltage oscillations of the FCs.

A symmetrical hybrid MLI for high-speed motor drive systems was presented in [101] as shown in Fig. 26, consisting of 36 switches, 12 capacitors, and 3 dc sources for generating nine voltage levels. It uses two cascaded three-level FCs to work as a multilevel dc link (MLDCL) generator stage, producing a five-level dc voltage waveform. Additionally, a full H-bridge is used as a polarity-changer. The MLDCL stage requires LV switches to operate at high frequencies, while HV switches are required for the low-frequency H-bridge. Using a reduced isolated dc source count and applying low-switching frequency for the four switches in each H-bridge are the main features of this MLI. However, the voltage balancing issues for capacitors under dynamic and nonideal conditions and the needs for HV switches that can withstand the full voltage of the dc-link are considered the key drawbacks.

Agrawal and Jain [102] have proposed a new unit acts as a building block for both LV and HV MLIs, as shown in Fig. 27(a),

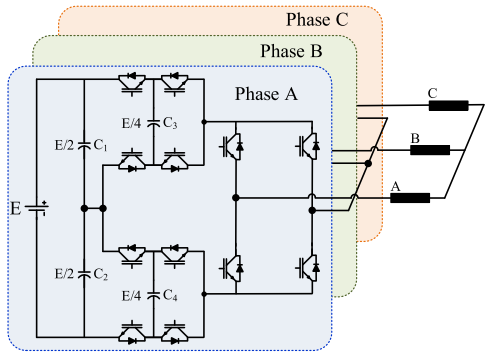


Fig. 26. Hybrid nine-level inverter for high-speed motor drives [101].

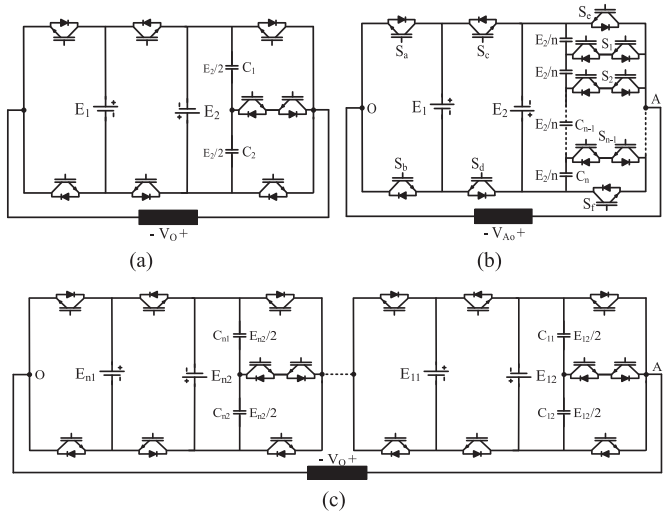


Fig. 27. MLI for interfacing renewable energy sources with low-, medium- and HV grids [102]. (a) Basic unit for generating 7-, 9-, and 11-level. (b) Two dc sources *N*-level configuration (leg A). (c) Multiple dc sources *N*-level configuration (leg A).

generating 9-, 7-, and 11- levels by using two dc voltage sources with ratios of 1:1, 2:1, and 2:3, respectively. It requires one bidirectional switch, six unidirectional switches and a voltage divider network formed by connecting two capacitors in series. Despite using only two dc sources, a high number of capacitors are required for generating N levels, as shown in Fig. 27(b). Accordingly, the proposed MLI suffers from the drawbacks mentioned above of using capacitors. Fig. 27(b) shows that the switches S_c and S_d must withstand a voltage of (E_1+E_2), being applicable for LV applications alone. The structure in Fig. 27(c) can be used in HV applications, but the advantage of using only two dc sources will be lost by cascading several units of two dc sources.

Alternatively, for medium-voltage applications, new MLI topologies were presented in [103] and [104]. Fig. 28 shows the schematic diagram of the topology in [103]. It is an upgraded circuit of the nested neutral point-clamped converter in [105]. The presented topology requires extra six switches and three FCs, but it can produce five voltage levels instead of only four levels in [105]. As observed in Fig. 28, using a significant number

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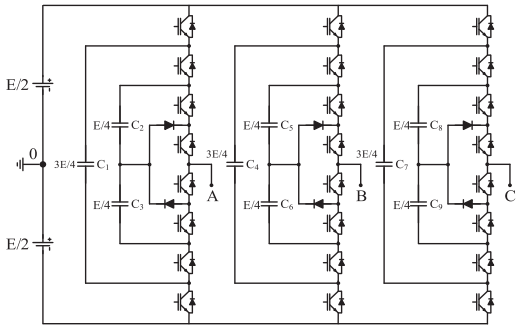


Fig. 28. Five-level VSI for medium-voltage applications [103].

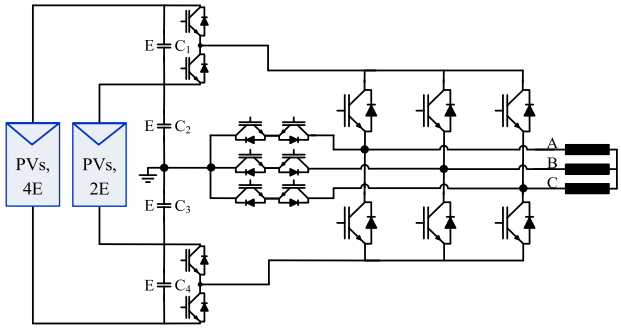


Fig. 30. Modified T-type three-level inverter for minimising CMV [107].

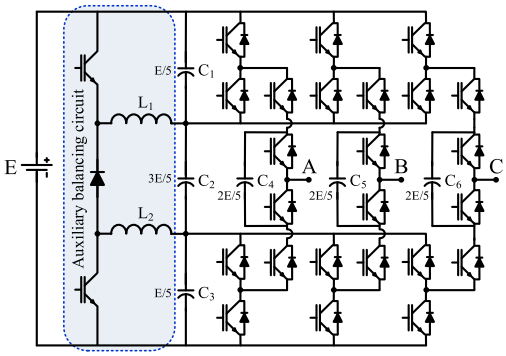


Fig. 29. Six-level MLI topology for medium-voltage applications [104].

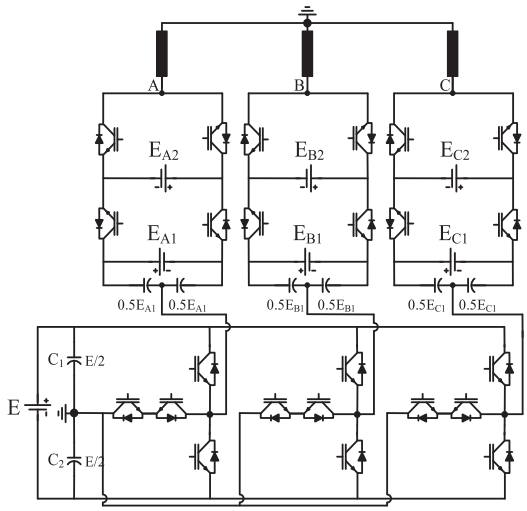


Fig. 31. Three-phase hybrid MLI for renewable energy [109].

of FCs and diodes, along with lack of modularity are the main limitations of this circuit. However, using less dc sources and having LV stress across the switches are its main features. In [104], Le and Lee have proposed a new six-level topology, being formed by combining three three-level FC legs with six two-level legs, as shown in Fig. 29. Despite using only one dc source, six capacitors and 24 switches are required for producing a three-phase voltage. While having a reduced count of switches and dc sources, the proposed inverter must use many capacitors that have diversified voltage ratings, requiring a voltage control for the flying and dc-link capacitors. Therefore, the authors have used the reported circuit in [106] for balancing the capacitors in the dc link, along with a precharging process for the FCs. For the proposed topology, it is important to mention that the auxiliary circuit for voltage balance of the dc-link capacitors is especially essential at a wide range of load power factor [104].

In transformerless PV systems, designing converters requires features, such as boosting capability, longer lifetime, and zero CMV [107]. To design a zero CMV converter, a modified T-type three-level inverter was presented in [107], merging the traditional T-type inverter with a dc-link that has four capacitors through two pairs of switches as shown in Fig. 30. Contrary to other solutions for eliminating the CMV in [108], the proposed topology has a low count of switches and capacitors and uses only 16 switches and four capacitors while eight capacitors and 24 switches are required in [108]. However, the TSV of the switches in [107] is higher than that in [108]. Further, for PV systems connected to a microgrid, a new hybrid modular MLI was proposed in [109]. Because of using a high number of dc sources, it is most applicable for PV farms where realizing dc voltage is easy. Fig. 31 shows the schematic diagram of its three-phase arrangement, in which a three-level T-type inverter works as the main stage, and a new four-level cell is connected in cascade for producing more levels. The new four-level cell is a modified full H-bridge and constructed from two capacitors, four switches, and two dc sources. The reduced switch count and the ability for operating in symmetrical or asymmetrical modes are the main features of this MLI. By employing the asymmetrical mode, the output level number will be increased while the component count will be the same. However, the topology must use different dc sources with proper voltage ratings, increasing the voltage stress across some switches. By using only one cell per phase in addition to the main stage, nine voltage levels can be achieved with 24 switches, eight capacitors, and seven symmetrical dc sources.

A new optimized multilevel topology was presented in [110], and Fig. 32 shows its configuration for producing N levels. Despite using the same main stage as topology in [109], i.e., T-type MLI, it has a different LG stage for enlarging the level number. Further, it is noted from Fig. 32 that the LG stage is subdivided into two identical units of one dc source and N_{HBs} half H-bridge cells. This topology could work as a symmetrical and asymmetrical MLI, requiring $(4N_{\mathrm{HBs}} + 12)$ switches and

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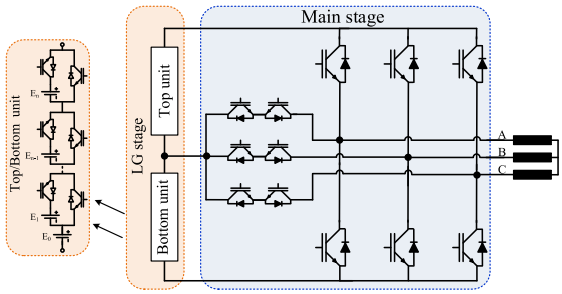


Fig. 32. Three-phase MLI topology with separate level and phase sequence generation part [110].

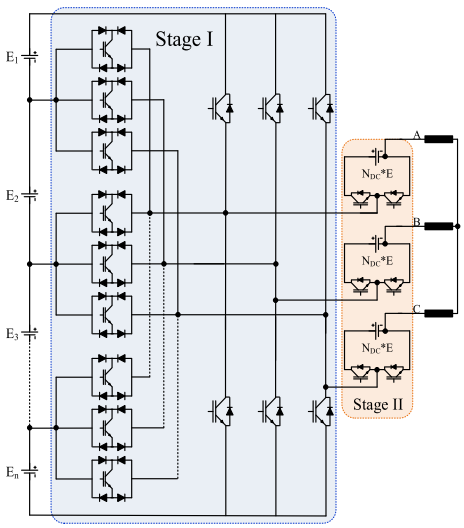


Fig. 33. Three-phase MLI using voltage doubling-unit [111].

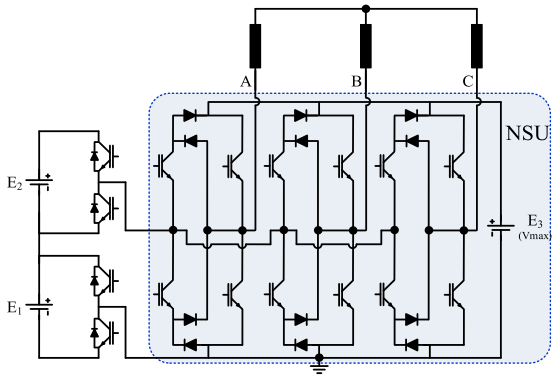


Fig. 34. Three-phase configuration based on cascaded HB [112].

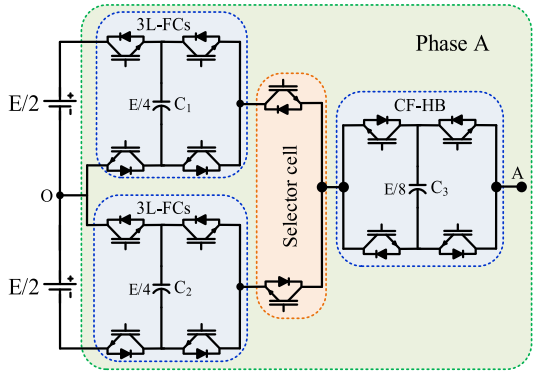


Fig. 35. One phase of a topology formed by stacking inverters of lower multilevel structures [113].

$(2N_{\mathrm{HBs}} + 2)$ dc sources for producing $(N_{\mathrm{HBs}} + 3)$ and $(2^{N\mathrm{HBs}} + 2)$ levels for symmetrical and asymmetrical operation, respectively. Diode-, capacitor-, inductor-free, and low component count are the main features of this circuit. In contrast, lack of modularity is considered the main demerit of this inverter, limiting the level count because of HV stress across the six unidirectional switches in T-type stage. These switches must withstand a voltage equal to the generated voltage by the LG stage.

Novel asymmetrical hybrid inverters in [111] and [112] can produce N levels with a reduced component count. The topology in [111] has two different stages, as shown in Fig. 33. Stage I consists of a traditional six-switch two-level inverter connected to dc-link through a bidirectional SN, in which each dc source is connected through one switch to one inverter leg. Stage II consists of three half H-bridge cells (one cell for each phase). Stage II is responsible for doubling the level count, so it is called a doubling unit. In spite of reducing the component count, it increases the rating voltage of components. As seen in Fig. 33, by using N_{DC} voltage sources of E, six switches must withstand $N_{\mathrm{DC}}{*}E$, and the other six switches in stage II have a rating more than $N_{\mathrm{DC}}{*}E$ and different ratings of the bidirectional switches based on its position. Alternatively, Fig. 34 shows the non-isolated-source based topology reported in [112], using stage II of topology in [111] to build a string of cascaded cells that are responsible for producing $(N-2)$ levels. Moreover, two extra levels are generated by a new structured unit (NSU). As shown in Fig. 34, the NSU is formed by three modified cells connected in parallel with a dc source of $V_{\max}$. The NSU can produce minimum and maximum levels of the generated voltage, i.e., 0 and $V_{\max}$, while the half H-bridge string generates the rest of levels. Generating four levels requires three dc sources of E, E, and $3E$ besides sixteen switches and twelve diodes. Although the number of levels is maximized in term of the component count, the TSV is dramatically increased in a similar way to the topology in [111].

The concept of generating a high number of levels by stacking capacitor-based full H-bridge cells was used in [113]. This concept is widely adopted for designing new circuits by using a low number of dc sources while increasing the number of FCs. For enlarging the number of levels, each group of the capacitors has a different voltage reference as compared to previous and subsequent groups. Therefore, additional voltage balancing algorithms are required for maintaining the capacitor voltages at the respective values. The nine-level circuit for the topology in [113] is depicted in Fig. 35, in which each phase has two three-level FCs, one selector cell, and one capacitor-fed H-bridge (CF-HB) unit. Producing nine levels requires two symmetrical dc sources (each of $0.5E$ volt), 42 switches (6, 24,

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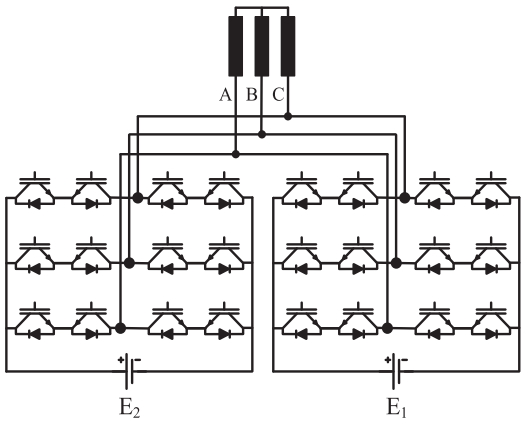


Fig. 36. Four-level topology for renewable energy grid integration [114].

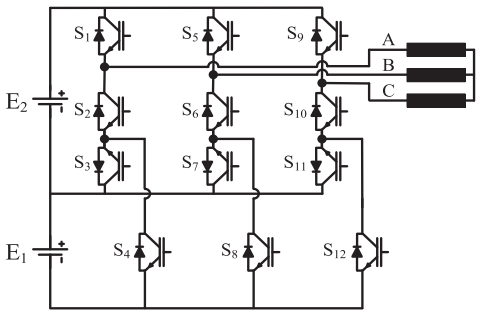


Fig. 37. Three-phase three-level MLI based on two-level VSI [115].

and 12 switches having blocking voltages of $0.5E$, $0.25E$, and $0.125E$, respectively), and nine capacitors (six of $0.25E$ and three of $0.125E$). It can generate N levels by increasing the number of FC and CF-HB cells, in addition to a modification in the selector cell.

Based on the conventional 2L-VSI, two MLIs were proposed in [114] and [115]. In [114], Amamra *et al.* presented a novel arrangement of two 2L-VSI. The proposed topology can generate N levels by using $N_{\rm DC}$ voltage sources and $(2(N_{\rm DC})^2 + 2N_{\rm DC})$ bidirectional switches, where each switch is built by connecting two unidirectional switches in the common-emitter configuration, reducing the required gate driver count. Fig. 36 shows its scaled-down circuit, being formed by connecting only two 2-level inverters in parallel while requiring 24 switches and two asymmetrical dc sources of E_1 and E_2 volt. Under the suggested PWM scheme by the authors, it can provide four levels $-E_1$, 0, E_2, and $(E_1{+}E_2)$ in the pole voltage and six-level line voltage. Using a high number of switches is one key limitation of this topology while using a low number of dc sources and having low requirements for the gate driver circuits are the main features. Contrary to connecting the 2L-VSIs as in [114], Salem *et al.*[115] have merged them in a distinct way for constructing a novel three-level unit as depicted in Fig. 37, in which two symmetrical dc sources and only twelve unidirectional switches are used. Several units with extra three switches must be cascaded for enlarging the number of levels. This topology has merits of using a low count of dc sources, and

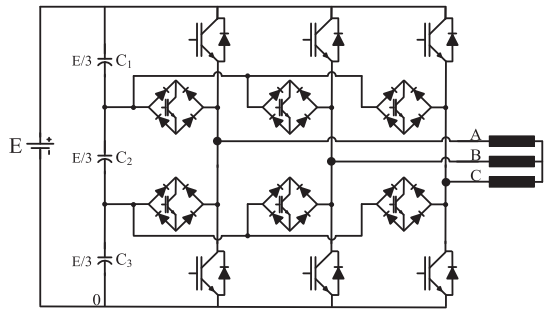


Fig. 38. Three-phase four-level inverter proposed in [116].

capacitor- and diode-free, being beneficial for control simplicity, compact design, long lifetime and low cost. However, a moderate TSV of the bottom three switches S_4, S_8, and S_{12} is the main limitation of this MLI.

A three-phase single source topology for standalone applications was presented in [116]. It is formed by three identical legs, sharing the same dc link. Each leg has two unidirectional switches and two bidirectional switches, as shown in Fig. 38. The dc-link consists of a single dc source accompanied by three voltage-divider capacitors C_1, C_2, and C_3. Controlling switches in each leg properly allows this topology to produce four levels 0, $E/3$, $2E/3$, and E in the pole voltage $V_{\rm A0}$, or result in seven levels of E, $2E/3$, $E/3$, 0, $-E/3$, $-2E/3$, and $-E$ in the line voltages. Using a single dc source, low count of active switches, and having only three ON-switch at any level are its main advantages. Its key disadvantages include using 3 capacitors, 24 power diodes, and HV stresses, which are equal to the full dc-link voltage across the six unidirectional switches while the six bidirectional switches must block 66.67% of the full dc-link voltage.

As highlighted earlier, the MLIs are salient candidates for several applications in both renewable energy systems and motor drives. Further, MLIs become a featured solution for improving the power quality in power systems. They can operate as static synchronous compensators (STATCOMs) and unified power quality conditioners (UPQCs), handling reactive power demand, harmonics compensation, and voltage disturbances (e.g., sag/swell). Flying-capacitor MLI (FCMLI), diode-clamped MLI (DCMLI), and cascaded H-bridge MLI (CHBMLI) are widely used to form multilevel-based STATCOMs [117]–[121]. Both FCMLIs and DCMLIs have dc-link shared among the three phases, improving the compensation of the negative-sequence currents as compared to the star-connected CHBMLI. These two topologies have a problem of poor modularity and using high capacitor and diode counts. The CHBMLIs have a remarkable feature of modularity, making them more attractive than FCMLIs and DCMLIs. However, connecting the CHB in a star-configuration reduces the compensation capability of the negative-sequence current. This drawback is solved by applying a delta-configuration of CHB, but this would boost the arming voltage of the converter, increasing the submodule count or rating the components [122].

Scalability and transformerless capability of the modular multilevel converter (MMC) make it reasonably competitive

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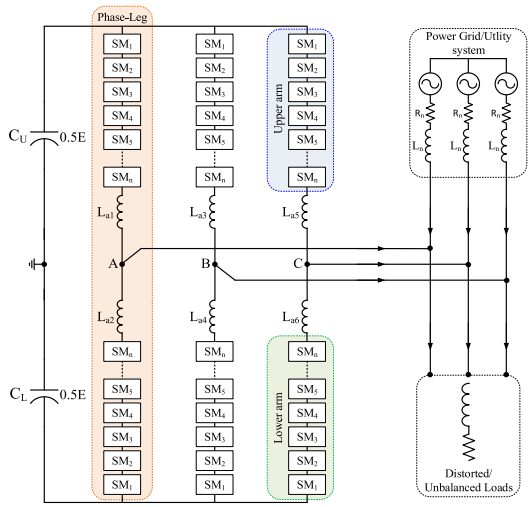


Fig. 39. MMC-based STATCOM configuration.

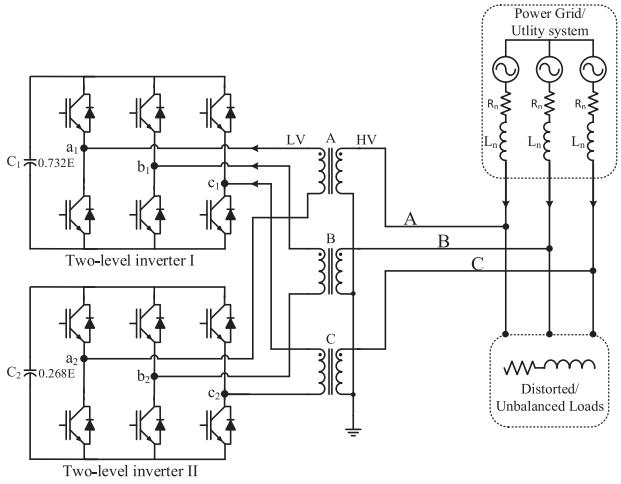


Fig. 41. STATCOM based on cascading two two-level VSIs in [128].

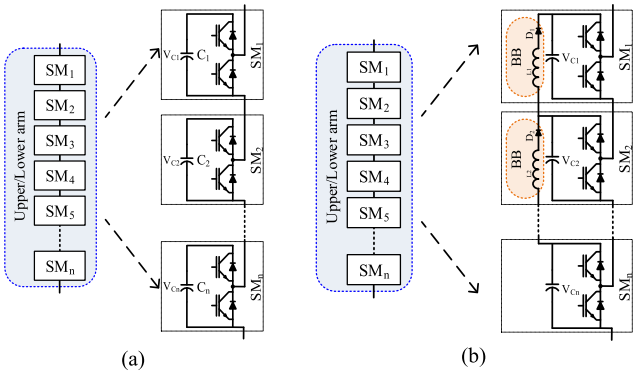


Fig. 40. Arm structures based on HB cells for MMC-based STATCOM. When capacitors voltage is balanced, $V_{Ci} = E/n$ where $i = 1, 2, \ldots, n$. (a) Conventional structure of an arm in MMC-based STATCOM. (b) Proposed diode-clamped arm structure in [122] for MMC-based STATCOM.

for replacing the conventional MLIs in HV STATCOM applications [123]. Fig. 39 shows the conventional MMC-based STATCOM configuration, consisting of three-phase legs connected to two bulk capacitors (C_U and C_L). Each phase has two arms (lower and upper arms) and two inductors (L_{a1} and L_{a2}). For constructing both arms, several submodules are cascaded, typically a FC connected to either half-bridge (HB) or full-bridge (FB). The arm inductors L_{a1}-L_{a6} are necessary for limiting the current during faults and reducing the harmonic content in the circulating current. Balancing the voltage of FCs is a significant challenge in STATCOM-based MMC, requiring complex control algorithms and a high number of voltage sensors [122]–[124]. Liu *et al.* [122] proposed a solution to keep the capacitor voltage in different submodules balanced, reducing the sensor count and computational burden in control algorithms. The conventional arm structure based on cascaded HB cells is depicted in Fig. 40(a), while Fig. 40(b) shows the proposed one. In the proposed structure, a balancing branch (BB), formed by a series connection of low-power rating inductor and diode, is added between the neighbored cells. The diodes are used to clamp the voltage of capacitors naturally from the bottom cell upwards. Using inductors is mandatory to suppress the current pulses during abnormal conditions, protecting the switches and reducing the diode current ratings. According to the proposed solution, only the voltage of the capacitor in either the top or bottom of each arm must be controlled and monitored. The remarkable features of simplifying voltage balancing control and low sensor count come with the cost of increasing the component count (diodes and inductors) as compared to the conventional MMC.

To synthesise a desired multilevel ac voltage, a large count of floating capacitors is required in the MMC-based STATCOM, in which electrolytic capacitors are normally used to fulfil the high-capacitance requirements for buffering energy variations. Besides the well-known disadvantages of using a large number of capacitors [125], the electrolytic ones have a higher failure rate than other components in the systems [125]–[127]. To lower capacitor count and voltage rating of switches while producing higher voltage levels, some transformer-based solutions were proposed in [128] and [129]. Babu and Fernandes [128] introduced a four-level STATCOM configuration based on cascading two conventional two-level inverters, as depicted in Fig. 41. Two corresponding legs of the two-level inverters are connected through one winding of a three-phase transformer. The LV windings are used for cascading the two inverters while the three windings of the HV side are connected to the grid terminals. To obtain a four-level operation, the voltages of the two dc-link capacitors are regulated to have asymmetrical values. One three-phase transformer is needed in addition to twelve switches and two capacitors. This topology has a simple structure and a low component count. However, the demerit of using a three-phase transformer (in term of size and cost) restricts its applicability, being more advantageous in low-capacity STATCOMs. A modified topology of the presented STATCOM configuration in [128], was proposed in [129]. Three two-level inverters and a three-phase transformer are used to construct the proposed STATCOM in Fig. 42. One leg in each inverter is used to connect the three inverters in a Y-configuration, while the remaining two legs are connected to different windings in the LV side of the transformer. This connection makes the applied ac

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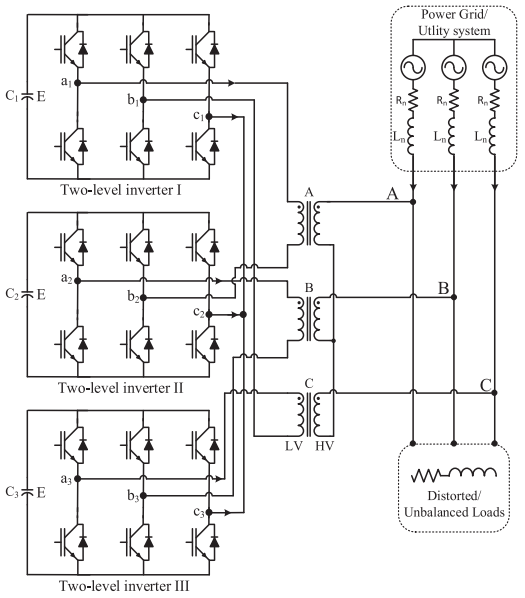


Fig. 42. STATCOM based on three two-level VSIs in [129].

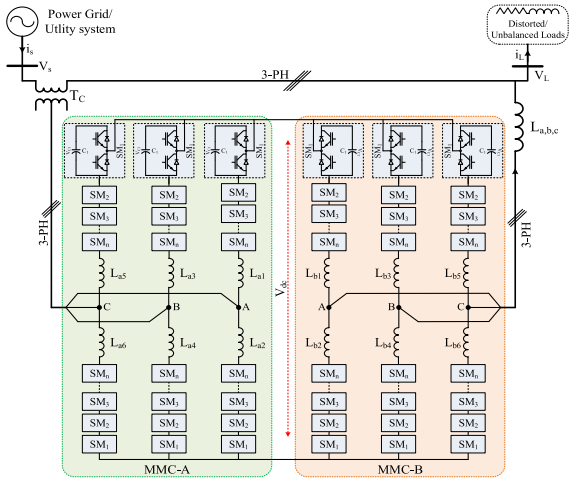


Fig. 43. Configuration of MMC-based UPQC in [137]–[139].

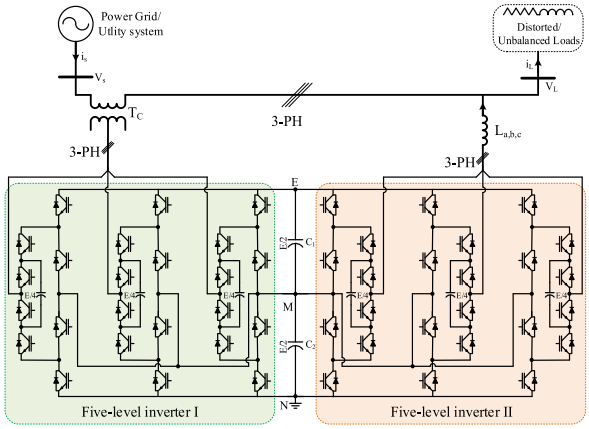


Fig. 44. Configuration of UPQC implemented by the back-to-back connection of two five-level inverters [140].

voltage of the transformer windings double the dc voltage across the capacitor. Under the regulation of the capacitor voltages at symmetrical values, the proposed configuration produces five voltage levels of $-2E$, $-E$, 0, E, and $2E$ across each transformer winding, requiring one three-phase transformer, three capacitors, and eighteen switches. As compared to [128], the proposed topology needs one extra two-level inverter (i.e., one capacitor and six switches). Consequently, the applied voltage across the transformer winding is increased from 1.33 to double the capacitor voltage while producing five levels instead of four, lowering both THD value and component ratings. It is worth mentioning that the topologies in [128] and [129] have been introduced for driving open-end winding induction motors [130], [131].

Another significant application of the MLIs in the field of power quality is constructing more competitive UPQCs. Briefly, UPQC consists of two compensators, in which the series compensator is responsible for handling voltage related issues (e.g., voltage sag/swell, flickers, etc.) and the shunt compensator is to tackle issues of harmonic and reactive power compensations [132]–[140]. Several configurations for UPQCs based on conventional MLI topologies were proposed in [133]–[136], suffering from a high component count or limited level count due to using many capacitors or diodes or transformers. The MMC concept was applied to obtain UPQCs with higher power levels [137]–[139]. Fig. 43 shows the UPQC based on two MMCs. The MMC-A acts as a series compensator, being connected to the grid through a series injection transformer (T_C), while three coupling inductors (L_a, L_b, and L_c) are used to interface the shunt compensator (i.e., MMC-B) to the grid. It is worth noting that the coupling inductors can be used for smoothing the currents. Attractive features, namely high-quality waveforms, fast current control, and easy scalability of voltage and current, are important in applying MMC to UPQC. On the other hand, using many floating capacitors as storage elements, increasing size and failure rates, is its main limitation for UPQCs.

Another MLI-based UPQC was proposed in [140], and the proposed configuration is shown in Fig. 44. It consists of two identical MLIs, being connected in back-to-back assembly. Each inverter requires 24 switches and 3 floating capacitors for producing five levels. Two capacitors C_1 and C_2 are used for constructing a dc-link with a middle point called M. As compared to the introduced diode-clamped UPQC in [136], the proposed UPQC configuration saves 36 diodes, but needs eight capacitors instead of four. Although both UPQC configurations require the same switch count, the TSV of switches in [140] is higher than that in [136]. Further, both must use a sophisticated control for balancing capacitors voltage at specific values.

III. Proposed Benchmark for Comparing MLI Topologies

A. Existing Factors for Comparing Multilevel Topologies

Over the past few years, several MLI topologies have been proposed for improving the power conversion efficiency, system reliability, power quality in several applications. The significant number and diversity of the proposed topologies allow the customers to select the suitable one to their needs, but selecting

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the best one is always a challenge. Different aspects and aims are set in a design process, for example, low semiconductors count, low passive elements, isolation features, boosting abilities, modularity, etc. To make the comparative process easier and more efficient for both industry and academia, two strategies have been presented in [34] and [35]. The strategy in [34] is based on the LSR for comparing different MLIs. As described in (1), the *LSR* is calculated by the number of levels *N* over the switch count ($N_{\rm SW}$), indicating number of levels generated by each switch. Accordingly, topologies with higher *LSR* are better than those with a lower one from the switch count point of view

$$\text{LSR} = \frac{N}{N_{\rm SW}}. \tag{1}$$

LSR cannot figure out other component counts, e.g. capacitors ($N_{\rm C}$), inductors ($N_{\rm L}$), diodes ($N_{\rm D}$), transformers ($N_{\rm TRF}$), dc sources ($N_{\rm DC}$), and other components ($N_{\rm X}$). To overcome this drawback, the CLF was proposed in [35] as a comparative factor. Instead of counting only switches, CLF is to count all the used components for producing one level, as calculated in (2). Therefore, it can be used to compare MLI topologies by the total component count. A reduced component circuit has a lower CLF

$$\text{CLF} = \frac{N_{\rm C} + N_{\rm D} + N_{\rm L} + N_{\rm SW} + N_{\rm DC} + N_{\rm TRF} + N_{\rm X}}{N}. \tag{2}$$

The proposed MLI topologies in [36]–[56], [58]–[83], [85], [86], [92], [95]–[97], [101]–[104], [107], [109]–[116], and [141]–[156] are compared together by using the two comparative factors LSR and CLF in terms of component count. The compared MLIs in this article are named from *T*1 to *T*120, in which the same reference can be seen in different categories because some authors have proposed two or more configurations in one publication. Tables I and II show comparisons for single-phase MLI topologies of single/symmetrical and asymmetrical dc sources in the literature while the three-phase MLIs are compared and given in Tables III and IV. The presented topologies were very diverse, in which some of them can generate *N* levels while the others were designed for a specific voltage level number. Therefore, to make a fair comparison, they are grouped based on the number of levels, for example, group A represents five-level topologies that use either symmetrical or single dc sources. The last row of each group highlights a topology that has the least component count. In the comparison, several aspects are adopted/assumed: each battery or PV string is counted as one dc source, and each winding of a coupled inductor is considered one inductor, input, and output filter components are discounted, a three-phase transformer is calculated as three single-phase transformers and the same for multiwinding/secondary transformers cases. The unidirectional switch is considered as the base for counting the switch number, so bidirectional ones are disassembled into their primary components.

Based on Tables I–IV, the drawbacks of using LSR for comparing MLIs have been solved by CLF. However, important factors like component ratings have been ignored when computing CLF values for the compared circuits since the CLF alone is not able to compare the used components in term of ratings. One device with a voltage rating of 10*E* has been equally counted as a device with the voltage rating of 0.5*E*. Consequently, a new indicator or method for comparing MLI topologies more accurately is very important for both industry and academia to select the best circuit in term of the component count.

B. Proposed Comparative Factor: Component for Each Level

In this section, a new method is proposed to compare MLI topologies. First, the MLI components are subdivided into two groups: semiconductors and passive elements. The semiconductor group includes switches and diodes while capacitors, inductors, and transformers are classified as passive elements. Second, for simplicity, the peak current passing through each component is assumed to be the same and equal to the load current. Further, the peak voltage (VPK) is considered as an indicator for the rating of the component.

For calculating the equivalent semiconductor count $NE_{\rm SEMI}$, the TSV ($\text{TSV}_{\rm SEMI}$) for $NE_{\rm SEMI}$ elements is calculated as in (3). Afterward, $NE_{\rm SEMI}$ is defined by $\text{TSV}_{\rm SEMI}$ and the base value of the voltage ($V_{\rm BASE}$) in (4). For the passive elements, several parameters, such as capacitance, inductance, and equivalent resistance, are used in the evaluation. Each topology has different specifications based on input/output waveforms or depending on facility conditions of research groups. In the proposed comparative strategy, the voltage is a dominant factor as the current has been assumed equal to the load current. The equivalent numbers of capacitors $NE_{\rm C}$, inductors $NE_{\rm L}$, transformers $NE_{\rm TRF}$, and dc sources $NE_{\rm DC}$ are calculated by (5)–(8), respectively. For example, if topology $T_{\rm X}$ requires two dc sources of *E* and 2*E* volt, the number of dc sources $N_{\rm DC}$ is 2, while the equivalent number $NE_{\rm DC}$ is equal to three ($NE_{\rm DC}$=(*E*+2*E*)/*E*). The same rule can be applied for the rest of the used components. The total equivalent component count $NE_{\rm TOTAL}$ and CEL are defined by (9) and (10), respectively

$$\text{TSV}_{\rm SEMI} = \sum_{i=1}^{N_{\rm SEMI}} \text{VPK}_{\rm i} \tag{3}$$

$$NE_{\rm SEMI} = \frac{\text{TSV}_{\rm SEMI}}{V_{\rm BASE}} \tag{4}$$

$$NE_{\rm C} = \frac{\sum_{i=1}^{N_{\rm C}} \text{VPK}_{\rm i}}{V_{\rm BASE}} \tag{5}$$

$$NE_{\rm L} = \frac{\sum_{i=1}^{N_{\rm L}} \text{VPK}_{\rm i}}{V_{\rm BASE}} \tag{6}$$

$$NE_{\rm TRF} = \frac{\sum_{i=1}^{N_{\rm TRF}} \text{VPK}_{\rm i}}{V_{\rm BASE}} \tag{7}$$

$$NE_{\rm DC} = \frac{\sum_{i=1}^{N_{\rm DC}} \text{VPK}_{\rm i}}{V_{\rm BASE}} \tag{8}$$

$$NE_{\rm TOTAL} = NE_{\rm SEMI} + NE_C + NE_L + NE_{\rm TRF} + NE_{\rm DC} \tag{9}$$

$$\text{CEL} = \frac{NE_{\rm TOTAL}}{N}. \tag{10}$$

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TABLE I
COMPONENT REQUIREMENT FOR SINGLE-PHASE MLIS IN [36]–[47], [49], [51]–[56], [59], [61]–[63], [65]–[67], [70]–[73], [75], [77], [80], [81], [83], [85], [86], [102], [141], AND [142]

	Topology	In	N	N_{DC}	N_{SW}	N_D	N_L	N_C	N_{TRF}	N_{TOTAL}	*LSR*	*CLF*
Group A	T120	[85]	5	1	8	6	4	4	0	23	0.63	4.60
	T38	[37]	5	2	8	4	2	3	0	19	0.63	3.80
	T119	[86]	5	1	8	3	2	4	0	18	0.63	3.60
	T48	[70]	5	1	12	0	0	4	0	17	0.42	3.40
	T59	[77]	5	1	10	0	0	4	0	15	0.50	3.00
	T34	[39]	5	2	4	4	2	2	0	14	1.25	2.80
	T37	[38]	5	2	4	4	2	2	0	14	1.25	2.80
	T54	[36]	5	1	6	3	1	2	0	13	0.83	2.60
	T47	[75]	5	1	6	2	0	3	0	12	0.83	2.40
	T52	[71]	5	2	8	0	0	2	0	12	0.63	2.40
	T43[a]	[65]	5	2	7	2	0	0	0	11	0.71	2.20
	T51	[72]	5	1	6	0	0	3	0	10	0.83	2.00
Group B	T49	[73]	7	1	16	0	0	3	0	20	0.43	2.85
	T58	[59]	7	1	8	4	0	3	0	16	0.88	2.29
	T30	[66]	7	1	7	2	0	3	0	13	1.00	1.86
	T45	[67]	7	3	10	0	0	0	0	13	0.70	1.86
	T65	[141]	7	1	8	0	0	4	0	13	0.88	1.86
	T110	[83]	7	1	9	0	0	3	0	13	0.78	1.86
	T24[a]	[62]	7	3	6	2	0	0	0	11	1.17	1.57
	T26[a]	[61]	7	3	8	0	0	0	0	11	0.88	1.57
	T46	[63]	7	3	7	1	0	0	0	11	1.00	1.57
Group C	T35	[39]	9	1	8	8	4	2	0	23	1.13	2.56
	T1	[43]	9	1	16	0	0	0	4	21	0.56	2.33
	T56	[56]	9	1	10	4	1	4	0	20	0.90	2.22
	T44[a]	[65]	9	4	9	4	0	0	0	17	1.00	1.89
	T110	[83]	9	1	12	0	0	4	0	17	0.75	1.89
	T33	[42]	9	1	12	0	0	3	0	16	0.75	1.78
	T36	[39]	9	1	6	4	2	2	0	15	1.50	1.67
	T17	[54]	9	1	8	0	0	2	4	15	1.13	1.67
	T40	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T41	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T42	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T53	[41]	9	1	10	0	0	3	0	14	0.90	1.56
	T55	[55]	9	1	9	2	0	2	0	14	1.00	1.56
	T2	[44]	9	1	10	0	0	3	0	14	0.90	1.56
	T3	[45]	9	1	10	0	0	3	0	14	0.90	1.56
	T111	[80]	9	4	10	0	0	0	0	14	0.90	1.56
	T25[a]	[62]	9	4	7	2	0	0	0	13	1.29	1.44
	T39	[40]	9	2	8	0	2	0	0	12	1.13	1.33
	T62	[102]	9	2	8	0	0	2	0	12	1.13	1.33
	T14	[52]	9	2	8	0	0	0	1	11	1.13	1.22
	T64	[142]	9	2	8	0	0	1	0	11	1.13	1.22
	T8	[49]	9	1	8	0	0	0	1	10	1.13	1.11
	T16	[53]	9	1	8	0	0	0	1	10	1.13	1.11
Group D	T117	[81]	15	1	26	0	0	7	0	34	0.58	2.27
	T46	[63]	15	7	13	3	0	0	0	23	1.15	1.53
	T5	[46]	15	1	8	0	0	2	3	14	1.88	0.93
	T13	[51]	15	1	8	0	0	0	2	11	1.88	0.73
Group E	T6	[47]	27	1	12	0	0	0	3	16	2.25	0.59
	T14	[52]	27	2	12	0	0	0	2	16	2.25	0.59
	T15	[52]	27	2	12	0	0	0	2	16	2.25	0.59

[a] Addressed for symmetrical mode alone, more details for their operation under asymmetrical mode (DC sources have asymmetrical values) can be found in [61], [62], and [65]. Only number of levels will be changed while using same component count.

The passive elements in the MLI topologies, such as capacitors and inductors, have distinctive natures as compared to other components since they store energy either in magnetic or electric fields. An additional comparative factor, namely stored energy factor (SEF), is proposed to take their stored energy (SE) into consideration when comparing topologies beside their equivalent numbers. The total stored energy (TE) of SE elements (N_{SE}) is calculated in (11) and used to obtain the proposed SEF in (12)

$$\mathrm{TE} = \sum_{i=1}^{N_{\mathrm{SE}}} \mathrm{SE_i} \tag{11}$$

$$\mathrm{SEF} = \frac{\mathrm{TE}}{\mathrm{TE_{BASE}}} \tag{12}$$

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TABLE II
COMPONENT REQUIREMENT FOR ASYMMETRICAL SINGLE-PHASE MLIS IN [48], [50], [51], [58], [60], [64], [66], [68], [69], [74], [76], [78]– [80], [82], [102], AND [143]

	Topology	In	N	N_{DC}	N_{SW}	N_D	N_L	N_C	N_{TRF}	N_{TOTAL}	*LSR*	*CLF*
Group F	T115	[74]	5	2	6	1	0	0	0	9	0.83	1.8
Group G	T61-a	[102]	7	2	8	0	0	2	0	12	0.88	1.71
	T4	[143]	7	2	8	0	0	0	0	10	0.88	1.43
Group H	T112	[68]	9	2	10	0	0	0	0	12	0.90	1.33
	T116	[82]	9	2	8	0	0	0	0	10	1.12	1.11
Group I	T63	[102]	13	4	16	0	0	4	0	24	0.81	1.85
	T61-a	[102]	13	2	14	0	0	5	0	21	0.93	1.62
	T19	[76]	13	4	10	0	0	0	0	14	1.30	1.08
Group J	T113	[69]	15	3	9	4	0	0	0	16	1.67	1.06
	T61-b	[102]	15	2	10	0	0	3	0	15	1.50	1.00
	T60	[143]	15	3	10	0	0	0	0	13	1.50	0.87
	T18	[79]	15	3	8	0	0	0	0	11	1.88	0.73
	T12	[51]	15	2	8	0	0	0	1	11	1.88	0.73
Group K	T22[a]	[60]	17	2	10	2	0	2	0	16	1.70	0.94
	T111	[80]	17	4	10	0	0	0	0	14	1.70	0.82
	T29	[64]	17	4	10	0	0	0	0	14	1.70	0.82
Group L	T61-b	[102]	19	2	12	0	0	4	0	18	1.58	0.95
	T7	[48]	19	2	10	2	0	0	2	16	1.90	0.84
	T9	[50]	19	2	12	0	0	0	2	16	1.58	0.84
Group M	T61-a	[102]	23	2	24	0	0	10	0	36	0.96	1.57
	T31	[66]	23	2	13	3	0	5	0	23	1.77	1.00
	T61-b	[102]	23	2	14	0	0	5	0	21	1.64	0.91
Group N	T63	[102]	25	8	32	0	0	8	0	48	0.78	1.92
	T61-a	[102]	25	2	26	0	0	11	0	39	0.96	1.56
	T32[a]	[78]	25	4	10	8	0	0	0	22	2.50	0.88
Group O	T6-b	[102]	31	2	18	0	0	7	0	27	1.72	0.87
	T28	[64]	31	6	14	0	0	0	0	20	2.21	0.65
Group P	T63	[102]	49	16	64	0	0	16	0	96	0.77	1.96
	T23[a]	[60]	49	3	14	3	0	3	0	23	3.50	0.47
	T11[a]	[51]	49	2	12	0	0	0	2	16	4.08	0.33
	T116	[82]	49	4	12	0	0	0	0	16	4.08	0.33
Group Q	T63	[102]	55	18	72	0	0	18	0	108	0.76	1.96
	T21	[58]	55	3	44	0	0	7	0	54	1.25	0.98
	T61-b	[102]	55	2	30	0	0	13	0	45	1.83	0.82

[a]Addressed for asymmetrical mode alone, more details for their operation under symmetrical mode (dc sources have symmetrical values) can be found in [51], [60],and [78]. Only number of levels will be changed while using same component count.

TABLE III
COMPONENTS REQUIREMENT FOR ASYMMETRICAL THREE-PHASE MLI TOPOLOGIES IN [102], [109]–[112], [114], [143], [149], AND [156]

	Topology	In	N	N_{DC}	N_{SW}	N_D	N_L	N_C	N_{TRF}	N_{TOTAL}	*LSR*	*CLF*
Group R	T81	[112]	4	3	16	12	0	0	0	31	0.25	7.75
	T82	[114]	4	2	24	0	0	0	0	26	0.17	6.50
Group S	T80	[111]	7	6	18	24	0	0	0	48	0.39	6.86
	T86	[102]	7	6	24	0	0	6	0	36	0.29	5.14
	T74	[143]	7	6	24	0	0	0	0	30	0.29	4.29
Group T	T81	[112]	10	9	28	12	0	0	0	49	0.36	4.90
	T79	[110]	10	8	24	0	0	0	0	32	0.42	3.20
Group U	T80	[111]	11	8	24	48	0	0	0	80	0.46	7.27
	T88	[102]	11	6	24	0	0	6	0	36	0.46	3.27
Group V	T80	[111]	15	10	30	72	0	0	0	112	0.50	7.47
	T75	[143]	15	9	30	0	0	0	0	39	0.50	2.60
Group W	T81	[112]	17	16	42	12	0	0	0	70	0.40	4.12
	T89	[156]	17	6	36	0	0	9	0	51	0.47	3.00
Group X	T80	[111]	19	12	36	96	0	0	0	144	0.53	7.58
	T85	[109]	19	13	36	0	0	14	0	63	0.53	3.32
Group Y	T81	[112]	31	30	70	12	0	0	0	112	0.44	3.61
	T76	[143]	31	12	36	0	0	0	0	48	0.86	1.55
Group Z	T71	[149]	33	4	36	0	0	6	3	49	0.92	1.48
	T90	[149]	33	6	36	0	0	6	0	48	0.92	1.45

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TABLE IV
COMPONENT REQUIREMENT FOR THREE-PHASE MLIs IN [39], [44], [45], [92], [95]–[97], [101]–[104], [107], [109], [110], [113], [115], [116], [141], [142], [144]–[148], AND [150]–[155]

	Topology	In	N	N_{DC}	N_{SW}	N_D	N_L	N_C	N_{TRF}	N_{TOTAL}	*LSR*	*CLF*
Group A1	T94	[95]	3	2	14	10	2	2	0	30	0.21	10.00
	T103	[96]	3	1	12	2	4	4	0	23	0.25	7.67
	T107	[150]	3	1	14	4	1	2	0	22	0.21	7.33
	T93	[107]	3	1	16	0	0	4	0	21	0.19	7.00
	T104	[97]	3	1	12	3	1	4	0	21	0.25	7.00
	T114	[116]	4[a]	1	12	24	0	3	0	40	0.58	5.71
	T118	[92]	3	1	12	0	0	2	0	15	0.25	5.00
	T96	[115]	3	2	12	0	0	0	0	14	0.25	4.67
Group B1	T97	[103]	5	2	24	6	0	9	0	41	0.21	8.20
	T108	[151]	5	1	21	12	0	5	0	39	0.24	7.80
	T77	[39]	5	2	12	12	6	2	0	34	0.42	6.80
	T99	[154]	5	2	20	6	0	2	0	30	0.25	6.00
	T69	[147]	5	2	24	0	0	0	3	26	0.21	5.80
	T100	[154]	5	2	20	0	0	2	0	24	0.25	4.80
	T105	[152]	5	1	18	0	0	4	0	23	0.28	4.60
	T67	[144]	5	1	16	0	0	2	2	19	0.31	4.20
	T109	[153]	5	1	15	0	0	3	0	19	0.33	3.80
	T66	[145]	5	1	12	0	0	2	2	15	0.42	3.40
Group C1	T78	[110]	6	8	24	0	0	0	0	32	0.25	5.33
	T102	[104]	6	1	24	0	0	6	0	31	0.25	5.17
Group D1	T98	[155]	7	2	36	0	0	9	0	47	0.19	6.71
	T106	[141]	7	1	24	0	0	8	0	33	0.29	4.71
Group E1	T91	[113]	9	2	42	0	0	9	0	53	0.21	5.89
	T95	[101]	9	3	36	0	0	12	0	51	0.25	5.67
	T72	[44]	9	1	30	0	0	9	3	40	0.30	4.78
	T73	[45]	9	1	30	0	0	9	3	40	0.30	4.78
	T83	[109]	9	7	24	0	0	8	0	39	0.38	4.33
	T101	[142]	9	6	24	0	0	9	0	39	0.38	4.33
	T87	[102]	9	6	24	0	0	6	0	36	0.38	4.00
	T70	[148]	9	2	16	0	0	0	6	18	0.56	2.67
Group F1	T78	[110]	15	26	60	0	0	0	0	86	0.25	5.73
	T84	[109]	15	13	36	0	0	14	0	63	0.42	4.20
Group G1	T84	[109]	21	19	48	0	0	20	0	87	0.44	4.14
	T68	[146]	21	1	48	0	0	0	12	49	0.44	2.90
Group H1	T69	[147]	49	24	156	0	0	0	3	180	0.31	3.73
	T92	[113]	49	3	84	6	0	18	0	111	0.58	2.27

[a]It can generate four levels, so it is inserted in the closest group, i.e., three-level inverters group.

where SE_i is the stored energy on a passive element i in a topology. TE_{BASE} is the total stored energy base value. The value of the TE_{BASE} can be the total stored energy of an interested or proposed topology.

The SEF can be calculated for different stored energy elements in a compared topology *T*x, indicating the stored energy in a percentage. SEF should be accompanied to the equivalent counts of the stored energy elements (i.e. NE_C and NE_L) when comparing *T*x with other topologies. These factors allow for a fairer comparison of topologies that contain stored energy elements. For example, two MLI topologies (T_A and T_B) use capacitors. T_A has two capacitors of 1 mF and voltage rating of 100 V, while T_B has three capacitors, (two of 0.25 mF and one of 0.5 mF) and all of the capacitors have voltage rating of 75 V. The equivalent count of the capacitor is defined by (5), and their SEFs are calculated by (11) and (12). The equivalent capacitor counts of T_A and T_B are 2 and 2.25, respectively, (V_{BASE} is selected at 100 V). The SEFs of T_A and T_B are 1 and 0.28 , respectively, (TE for T_A is "$2*0.5*1e^{-3}*100^2$" and for T_B is "$(2*0.5*0.25e^{-3}*75^2) + (0.5*0.5e^{-3}*75^2)$", TE_{BASE} is selected to be T_A stored energy). Accordingly, T_A has a less equivalent count of capacitors (2 instead of 2.25) as compared to T_B, but T_B has a lower SEF (0.28 instead of 1). Although the topology T_B requires a higher equivalent capacitor count, the capacitors store 28.1% of the stored energy in T_A, affecting the cost and size of the capacitors. It is worth mentioning that the same procedure can be applied to inductors as well.

To verify the effectiveness of the proposed factor CEL over the existing factor in ranking MLIs in term of component counts, five-level topologies *T*99, *T*100, CHB, NPC, and FC are selected in a comparative study as given in Table V. CHB, NPC, and FC are the conventional MLIs, while *T*99 and *T*100 are novel MLI topologies in [154]. A fair comparison among the selected topologies can be achieved because both number and value of the output voltage levels are the same for all of them (i.e. five levels of -0.25*E*, -0.5*E*, 0, 0.25*E*, and 0.5*E* volt). Table V also gives the voltage rating/stress for all components in the case-study topologies.

Topology *T*99 shown in Fig. 45 is selected as an example to clarify the CEL calculation. It consists of two dc sources, twenty switches, two capacitors, and six diodes. It requires eight switches with a voltage rating of 0.25*E* and twelve switches

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TABLE V
USING CLF AND CEL FOR COMPARING THE FIVE-LEVEL INVERTERS IN [154] AND THE THREE BASIC MLI TOPOLOGIES

Topology	DC sources			Switching devices			Diodes			Capacitors			Existing method		Proposed method	
	E/4	E/2	E	E/4	E/2	E	E/4	E/2	3E/4	E/4	E/2	3E/4	N_{TOTAL}	CLF	NE_{TOTAL}	CEL
T99	0	2	0	8	12	0	0	6	0	2	0	0	30	6	12.5	2.5
T100	0	2	0	8	6	6	0	0	0	2	0	0	24	4.8	12.5	2.5
CHB	6	0	0	24	0	0	0	0	0	0	0	0	30	6	7.5	1.5
NPC	0	0	1	24	0	0	6	6	6	4	0	0	47	9.4	17	3.4
FC	0	0	1	24	0	0	0	0	0	7	3	3	38	7.6	12.5	2.5

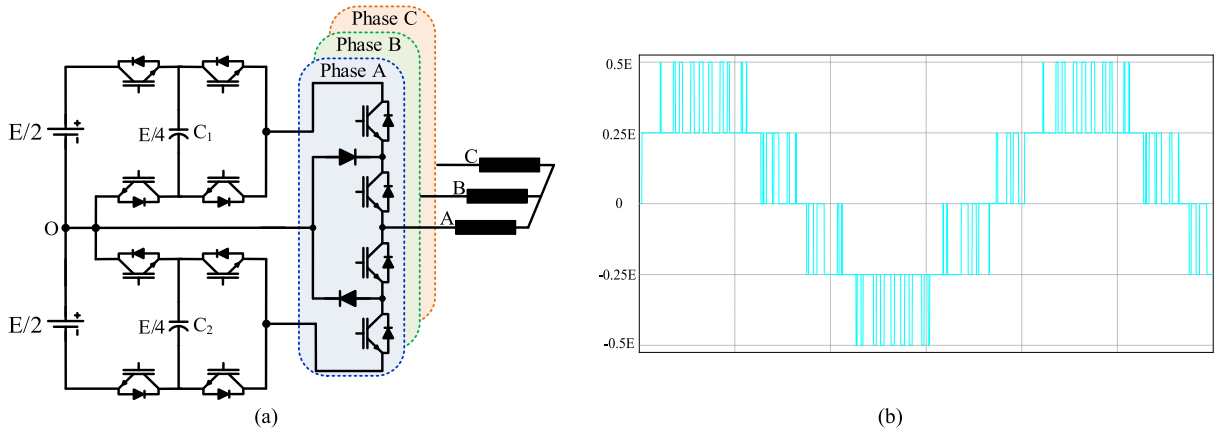


Fig. 45. Five-level three-phase topology *T*99 [154]. (a) Circuit configuration. (b) Output pole voltage for the compared MLI circuits in Table V.

TABLE VI
CALCULATION OF THE SEF FOR THE FIVE-LEVEL INVERTERS IN [154] AND THE THREE BASIC MLI TOPOLOGIES

Topology	Capacitors[a]			Stored energy factor calculation		
	E/4	E/2	3E/4	TE_{BASE}	TE	SEF
T99	2	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ (C_{A1}+C_{A2})$	1
T100	2	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ (C_{B1}+C_{B2})$	$(C_{B1}+C_{B2})/(C_{A1}+C_{A2})$
CHB	0	0	0	$E^2/32\ (C_{A1}+C_{A2})$	0	0
NPC	4	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ \sum_{i=1}^{4} C_{Ci}$	$\sum_{i=1}^{4} C_{Ci}\ /(C_{A1}+C_{A2})$
FC	7	3	3	$E^2/32\ (C_{A1}+C_{A2})$	$0.4375E^2 \sum_{i=1}^{13} C_{Di}$	$14 \sum_{i=1}^{13} C_{Di}\ /(C_{A1}+C_{A2})$

[a] C_{A1} and C_{A2} are the capacitors in T_{99}. C_{B1} and C_{B2} are the capacitors in T_{100}. C_{C1}, C_{C2}, C_{C3}, and C_{C4} are the capacitors in NPC. C_{D1}, C_{D2}, ... C_{D12}, and C_{D13} are the capacitors in FC.

with 0.5*E*, in addition to six diodes with a rating of 0.5*E* and two 0.25*E* capacitors. It does not have any transformers or inductors. For calculating the equivalent semiconductor count, NE_{SEMI}, first (3) is used for obtaining TSV_{SEMI} value, and then (4) is used to define NE_{SEMI}. TSV_{SEMI} is $11E$ ($= 8{*}0.25E{+}12{*}0.5E{+}6{*}0.5E$), so the value of NE_{SEMI} is 11. Using (5) and (8), NE_C and NE_{DC} can be calculated as ((0.25*E*+025*E*)/*E*) and ((0.5*E*+05*E*)/*E*), respectively. Using (9) and the obtained values of NE_{SEMI}, NE_{DC} and NE_C, results in the total component count of 12.5. Finally, CEL is calculated by using (10) to be 2.5. For the *T*100, CHB, NPC, and FC, the same procedure can be repeated.

In Table V, the differences between the existing method and the proposed one can be well observed. For example, in T99, the CLF factor results in the total component count N_{TOTAL} of 30 regardless of their voltage rating while NE_{TOTAL} is only 12.5 when using CEL factor. Without considering the component voltage rating or based on CLF values alone, the CHB requires more components than those in T100 since its CLF is higher than that of *T*100. However, when considering the voltage rating

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by the proposed indicator CEL, the total equivalent component count of the CHB is lower than that of *T*100 since the CEL of CHB is smaller than that of *T*100.

As mentioned before, in addition to the equivalent numbers of the used components in each topology to find CEL values, the SEF is recommended for a better description of stored energy elements in the compared topologies. Table VI gives the total energy TE and SEF for each topology based on (11) and (12). It is worth noting that the listed SEFs are a function of the utilized capacitors in the circuits, and not given as numerical values. Obtaining the numerical values requires detailed parameters of rated power, operating voltage, switching frequency, and voltage ripple, etc. It is important to consider all parameters that affect the stored energy element selection during the design process, when using SEF for obtaining a fairer comparison.

The comparison suggests that each topology should be evaluated by some of these factors, i.e. NE_{SEMI}, NE_{DC}, NE_{C}, NE_{L}, NE_{TRF}, SEF, and CEL, to highlight its merits, allowing for finding the most suitable application. For example, in PV farms, NE_{DC} is less important than that in motor drives while NE_{C}, NE_{L}, NE_{TRF}, and SEF should be reduced for more compact designs. For control simplicity, NE_{SEMI} and NE_{C} have the salient effects as compared to other factors. Finally, the CEL factor is the most important for having a reduced component count regardless of distinct features in each topology.

IV. Conclusion

This article presented a review study for the recently developed topologies in terms of construction, salient features and limitations, giving guidelines to further improve the current multilevel topologies more efficiently and compactly. A detailed comparison in terms of switch, diode, capacitor, inductor, and transformer count was performed and systematically summarized in tables. New comparative factors—CEL and SEF were introduced to compare MLI topologies more effectively. A comparative study was presented to verify the usefulness of the proposed factors for comparing MLIs, making it easier in evaluating newer topologies in the future.

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