Computationally Efficient Model Predictive Control With Fixed Switching Frequency of Five-Level ANPC Converters

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***Abstract*—This article proposes a fixed switching frequency (FSF)-based improved model predictive control (MPC) for a five-level active neutral-point clamped (5L-ANPC) converter. Compared to the conventional MPC for 5L-ANPC converter, the proposed MPC significantly reduces the computational burden while ensuring the balance of dc-link and flying capacitor voltages. The proposed MPC optimally selects the control voltage vectors to reduce common mode voltage (CMV), leading to a small CMV of the converter. Using three voltage vectors action per control cycle in MPC, FSF is achieved. Steady-state and dynamic performances of the proposed MPC have been evaluated by experiments. The results verify the feasibility and effectiveness of the proposed MPC method.**

***Index Terms*—Balance of capacitor voltages, five-level active neutral-point clamped (5L-ANPC) converter, fixed switching frequency (FSF), model predictive control (MPC), redundant switching states.**

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I. Introduction

FOR decades, three traditional types of multilevel circuit topologies; i.e., the flying capacitor's (FC) structure, neutral-point clamped (NPC) structure, and cascaded H-bridges (CHB) structure [1]–[5]; are commonly used in power converters. On one hand, the component counts of the FC and NPC will dramatically increase as the number of output voltage levels increases. On the other hand, CHB requires many isolated dc sources in the power converter. To overcome the drawbacks of the aforementioned topologies, many novel multilevel structures have been presented in recent years. Among the novel topologies, the five-level active neutral-point clamped (5L-ANPC) converter inherits the advantages of the five-level NPC and the five-level FC structures [6], [7]. Compared with the five-level NPC, the 5L-ANPC only needs one dc-link neutral-point (NP) voltage to be controlled, significantly simplifying the control complexity. Therefore, the 5L-ANPC is considered as a promising multilevel circuit structure for medium/high voltage applications.

To effectively control the three-phase 5L-ANPC (3P-5L-ANPC), the most utilized method is space vector pulse width modulation (SVPWM) technique or carrier-based pulsewidth modulation modified as pulse width modulation (PWM) technique [8]–[10]. However, for the 3P-5L-ANPC, there are 125 voltage vectors and 96 small triangle sectors, which complicates the control of 5L-ANPC by utilizing SVPWM [9], [10]. It is difficult to simultaneously achieve current tracking, reducing the common mode voltage (CMV), balancing the dc-link capacitor voltages (DCVs), and flying capacitor voltages (FCVs) when the carrier-based PWM technique is applied in the 3P-5L-ANPC.

Recently, model predictive control (MPC) has widely been utilized in industrial applications due to easily including different constraints. Generally, MPC can be classified as finite control set model predictive control (FCS-MPC) and continuous control set model predictive control (CCS-MPC). CCS-MPC calculates the voltage reference, then realizes by sinusoidal pulse width modulation (SPWM) or SVPWM with fixed switching frequency (FSF) performance. However, the CCS-MPC has heavy computational burden once constraints are considered. For the FCS-MPC, it can be further divided into optimal switching vector MPC (OSV-MPC) and optimal switching sequence MPC

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(OSS-MPC) in terms of the nature of the input constraint [11]–[13]. OSV-MPC evaluates every switching state of the converter in its cost function. The one that minimizes the cost function will be chosen as the optimal switching state and utilized in the next control cycle. Compared with the traditional PWM methods, OSV-MPC owns many merits such as multiobjective control without PWM blocks, no proportional integral (PI) controller, and fast/robust dynamic response. Therefore, OSV-MPC has attracted much attention and is considered as a promising control method for power electronic converters [14]–[18]. However, the number of switching states that need to be evaluated in OSV-MPC exponentially increases as the output voltage level increases. For three-phase converters, there are 27 (3^3) switching states for a three-level NPC converter, 216 (6^3) switching states for a four-level nested neutral-point clamped (NNPC) converter [19], 512 (8^3) switching states for a 5L-ANPC converter [20], and 1331 (11^3) switching states for a seven-level converter [21]. Obviously, the large number of switching states in multilevel inverters makes the real-time implementation of OSV-MPC algorithm very difficult [19]. Therefore, one of the main challenges for OSV-MPC is how to cut down the computational burden. In order to improve the computational efficiency, enhanced OSV-MPC algorithms have been reported for different three-phase three-level structures [23]–[25], four-level FC converters [26], and seven-level CHB static synchronous compensation device (STATCOM) [24]. Similarly, an efficient MPC algorithm for the three-phase four-level hybrid-clamped converter has been proposed in [28], which chooses 64 switching states instead of 512 switching states with the same output voltage level compared to the conventional MPC algorithm. However, it is noted that the aforementioned MPC approaches utilize one voltage vector in every sampling cycle, leading to variable switching frequency (VSF). Noticeably, VSF greatly increases the difficulty of the load filter design.

Several attempts have been made to address the VSF issue. In general, the current MPC methods with FSF can be categorized into two groups, i.e., the two-voltage vector and multiple voltage vector groups. The first group has been presented in [29] and [30] for two-level converters with reduced current ripples. Different multiple voltage vector FSF MPC algorithms belong to the second group, which have been presented to further reduce output current ripples and improve system performance in [31]–[36]. Similar ideas can also be extended to single-phase converters with the enhanced steady-state performance in [37]–[40]. Nevertheless, the existing FSF MPC methods only focus on the control of two-level or three-level converters. Few studies have been reported on the control of 5L-ANPC using MPC algorithms with the FSF. When the converter voltage level extends from two/three to five in an ANPC, it becomes very challenging to realize the FSF using MPC due to the large number of switching states.

Recently, different OSV-MPC algorithms for the 5L-ANPC have been studied. In [41], MPC for the 5L-ANPC utilized in medium voltage drives has been proposed, which achieves fast torque response with high quality of stator/rotor currents. In [42] and [43], improved OSV-MPC algorithms for the single-phase 5L-ANPC have been presented, which achieve the simultaneous

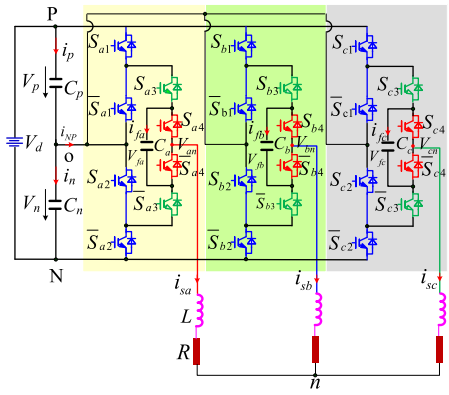


Fig. 1. Topology of the 3P-5L-ANPC.

control of DCVs, FCVs, and output currents in one control loop. Similarly, efficient OSV-MPC algorithms for the 3P-5L-ANPC have been presented with tracking current references, balancing DCVs and FCVs in [44] and [45]. However, for the above-mentioned MPC algorithms applied in the 5L-ANPC, there is only one voltage vector action during every control cycle, leading to VSF. To achieve FSF control for the 5L-ANPC, a two-stage MPC based on the deadbeat control and phase-shifted PWM has been presented in [46], which realizes the FSF control. To address the drawbacks of the above-mentioned MPC methods, an efficient MPC with FSF for 5L-ANPCs has been proposed. The main contributions are summarized as follows.

1) An efficient MPC with FSF for the 5L-ANPC is proposed, which generally contains three stages. The first stage chooses one of six medium voltage vectors with the minimum cost function for tracking current references. The second stage selects those candidate voltage vectors located at the same sector with the first-stage optimal medium voltage vector. The third stage balances DCVs and FCVs by selecting proper redundant switching states. Thus, compared with the conventional FSF MPC method in [36], the number of triangular sector evaluations significantly reduces from 96 to 16.
2) Weighting factors are eliminated for the proposed MPC, which avoids the tedious tuning process of weighting factors. DCVs and FCVs of the 5L-ANPC are balanced by choosing redundant switching states.
3) The proposed MPC abandons voltage vectors with high CMVs, and the CMV amplitude is limited to one-sixth of the dc-link input voltage. Therefore, the CMV and the leakage currents for the 5L-ANPC can be reduced.
4) Multiple objectives including tracking current references, balancing DCVs and FCVs, reducing the CMV, and FSF control are simultaneously achieved without heavy computational burden for the 5L-ANPC.

II. Converter Topology and Operational Principle

The topology of a 3P-5L-ANPC is depicted in Fig. 1. V_d is the dc-link input voltage, V_p and V_n are the upper and lower DCVs, respectively. i_p and i_n denote the currents of the dc-link

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TABLE I
SWITCHING COMBINATIONS OF LEG-A

S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{ao}	i_{NP}	i_{fa}	States
0	0	0	0	$-V_d/2$	0	0	$\mathbf{SS_{a0}}$
0	0	0	1	$-V_d/4$	0	$-i_{sa}$	$\mathbf{SS_{a1}}$
0	0	1	0	$-V_d/4$	i_{sa}	i_{sa}	$\mathbf{SS_{a2}}$
0	0	1	1	0	i_{sa}	0	$\mathbf{SS_{a3}}$
1	1	0	0	0	i_{sa}	0	$\mathbf{SS_{a4}}$
1	1	0	1	$V_d/4$	i_{sa}	$-i_{sa}$	$\mathbf{SS_{a5}}$
1	1	1	0	$V_d/4$	0	i_{sa}	$\mathbf{SS_{a6}}$
1	1	1	1	$V_d/2$	0	0	$\mathbf{SS_{a7}}$

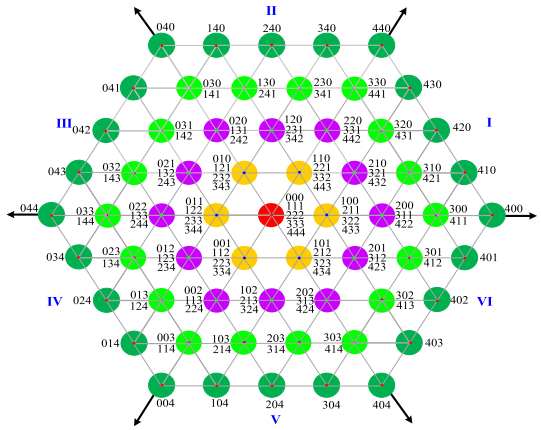


Fig. 2. Complete voltage vectors in the stationary reference frame.

upper and lower capacitors, respectively. V_{fx} ($x = a, b, c$) denotes the phase-x FCV. i_{sx} ($x = a, b, c$) represents the phase-x output current, and i_{fx} ($x = a, b, c$) is the phase-x FC current. C_p and C_n are the dc-link upper and lower capacitors, respectively. C_x ($x = a, b, c$) represents the phase-x FC. L and R indicate the load inductor and resistance. As seen in Fig. 1, the 3P-5L-ANPC consists of three legs, which are expressed as Leg-A, Leg-B, and Leg-C, respectively. Each leg contains eight power switches. Take Leg-A as an example, two basic rules should be followed.

1) Switches S_{a1} and $\overline{S_{a1}}$, S_{a2} and $\overline{S_{a2}}$, S_{a3} and $\overline{S_{a3}}$, S_{a4} and $\overline{S_{a4}}$ work in the complementary mode.
2) Switches S_{a1} and S_{a2} should be switched ON or OFF simultaneously.

The same principle can apply to Leg-B and Leg-C.

Assuming the upper and lower DCVs are controlled to be around $V_d/2$ and the FCVs are regulated around $V_d/4$, the switching states of Leg-A are listed in Table I. Each leg generates five levels in the output voltage, denoted as "$-V_d/2$," "$-V_d/4$," "0," "$V_d/4$," and "$V_d/2$." The five levels are corresponding to eight switching states. Therefore, for a 3P-5L-ANPC, it produces 125 (5^3) voltage vectors corresponding to 512 (8^3) switching states. Fig. 2 depicts all voltage vectors. "0," "1," "2," "3," and "4" are used to represent the five voltage levels, which are "$-V_d/2$," "$-V_d/4$," "0," "$V_d/4$," and "$V_d/2$," respectively.

From Table I, it is clearly observed the following.

1) Switching states $\mathbf{SS_{a0}}$ and $\mathbf{SS_{a7}}$ have no impact on DCVs and FCVs.
2) $\mathbf{SS_{a3}}$ and $\mathbf{SS_{a4}}$ output the same voltage with the same impact DCVs and FCVs.
3) $\mathbf{SS_{a1}}$ ($\mathbf{SS_{a2}}$) and $\mathbf{SS_{a5}}$ ($\mathbf{SS_{a6}}$) are considered as the redundant switching states.

They generate the same output voltage but have different effects on DCVs and FCVs. By properly selecting the redundant switching state, DCVs and FCVs can be balanced. The balancing mechanism is analyzed in detail in Section III.

III. FSF MPC ALGORITHMS

A. Mathematical Model of 3P-5L-ANPC

From Fig. 1, the dynamic equations of three output voltages are derived as

$$V_{xo} = L di_{sx}/\mathrm{d}t + Ri_{sx} + V_{no} \ \ (x = a, b, c) \tag{1}$$

where V_{xo} means the output voltage with respect to the reference point O in Fig. 1. The voltage V_{no} represents the CMV.

Due to fact that the sum of the three-phase output currents is zero, the CMV V_{no} is written as

$$V_{no} = (V_{ao} + V_{bo} + V_{co})/3. \tag{2}$$

In order to express output voltages with switching states, the switching state S_i ($i = a, b, c$) is defined as

$$\begin{cases} V_{io} = -V_d/2 & \text{if } S_i = 0 \\ V_{io} = -V_d/4 & \text{if } S_i = 1 \\ V_{io} = 0 & \text{if } S_i = 2 \\ V_{io} = V_d/4 & \text{if } S_i = 3 \\ V_{io} = V_d/2 & \text{if } S_i = 4 \end{cases}. \tag{3}$$

On the basis of (3), the output voltage can be obtained as

$$V_{io} = V_d(S_i - 2)/4. \tag{4}$$

Substituting (4) into (2), the CMV V_{no} is written as

$$V_{no} = (S_a + S_b + S_c - 6)V_d/12. \tag{5}$$

Substituting (5) into (1), the predictive output current $i_{sx}(k+1)$ at the $(k+1)$th sampling time is obtained as

$$\begin{cases} i_{sa}(k+1) = i_{sa}(k) + T_s(S_{as}(k)V_d - Ri_{sa}(k))/L \\ i_{sb}(k+1) = i_{sb}(k) + T_s(S_{bs}(k)V_d - Ri_b(k))/L \\ i_{sc}(k+1) = i_{sc}(k) + T_s(S_{cs}(k)V_d - Ri_{sc}(k))/L \end{cases} \tag{6}$$

where T_s means the sampling period. Switching function $S_{as}(k)$, $S_{bs}(k)$, and $S_{cs}(k)$ are obtained as

$$\begin{cases} S_{as} = (2S_a(k) - S_b(k) - S_c(k))/12 \\ S_{bs} = (-S_a(k) + 2S_b(k) - S_c(k))/12 \\ S_{cs} = (-S_a(k) - S_b(k) + 2S_c(k))/12 \end{cases}. \tag{7}$$

Thus, the phase-x ($x = a, b, c$) output voltage is written as

$$\begin{cases} V_{an} = V_{dc}(2S_a(k) - S_b(k) - S_c(k))/12 \\ V_{bn} = V_{dc}(-S_a(k) + 2S_b(k) - S_c(k))/12 \\ V_{cn} = V_{dc}(-S_a(k) - S_b(k) + 2S_c(k))/12 \end{cases}. \tag{8}$$

As demonstrated in (6), the behavior of output currents can be controlled by choosing proper switching states of the converter. Meanwhile, the discrete-time model of FCVs at the $(k+1)$th sampling time can be derived as

$$V_{fx}(k+1) = T_s i_{fx}(k)/C_x + V_{fx}(k) \ \ (x = a, b, c). \tag{9}$$

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As shown in Fig. 1, FCVs are obtained by switching states and output currents. Combining (9), it is written as

$$V_{fx}(k+1) = T_s\left(S_{x3} - S_{x4}\right) i_{sx}/C_x + V_{fx}(k)\ (x = a, b, c). \tag{10}$$

From (10), it can be understood that measuring FC currents can be avoided. Similarly, the predictive model of DCVs is expressed as

$$\begin{cases} V_p(k+1) = V_p(k) + T_s i_p(k)/C_p \\ V_n(k+1) = V_n(k) + T_s i_n(k)/C_n \end{cases}. \tag{11}$$

As seen in Fig. 1, output currents of the 3P-5L-ANPC will flow through the NP when the power switches $\overline{S_{x1}}$ and S_{x3} are ON or the power switches $\overline{S_{x3}}$ and S_{x1} are ON. Therefore, the NP current (i_{NP}) is expressed as

$$\begin{aligned} i_{NP} = {} & (S_{a1} + S_{a3} - 2S_{a1}S_{a3}) i_{sa} \\ & + (S_{b1} + S_{b3} - 2S_{b1}S_{b3}) i_{sb} \\ & + (S_{c1} + S_{c3} - 2S_{c1}S_{c3}) i_{sc}. \end{aligned} \tag{12}$$

As shown in Table I, the power switch S_{x1} ($x = a$, b, c) and S_{x2} ($x = a$, b, c) are turned ON or OFF at the same time. Thus, (11) can be further simplified as

$$i_{NP} = \left|S_{a1} - S_{a3}\right| i_{sa} + \left|S_{b1} - S_{b3}\right| i_{sb} + \left|S_{c1} - S_{c3}\right| i_{sc}. \tag{13}$$

As can be seen in Fig. 1, currents flowing through DCVs are obtained as follows:

$$\begin{cases} i_p = C_p(dV_p/dt) = i_n + i_{NP} \\ i_n = C_n(dV_n/dt) = C_n(d(V_d - V_p)/dt) \end{cases} \tag{14}$$

assuming that the DCV keeps constant and the dc-link upper capacitor C_p is equal to the dc-link lower capacitor C_n. On the basis of (14), the relationship between dc-link capacitor currents and the NP current is written as

$$\begin{cases} i_p = -i_n \\ i_p = i_{NP}/2 \\ C_p = C_n = C_{\mathrm{dc}} \end{cases} \tag{15}$$

where C_{dc} is the dc-link capacitor.

According to (11), (12), and (15), the predictive model of DCVs is written as

$$\begin{cases} V_p(k+1) = V_p(k) \\ +T_s(\left|S_{a1} - S_{a3}\right| i_{sa} + \left|S_{b1} - S_{b3}\right| i_{sb} \\ + \left|S_{c1} - S_{c3}\right| i_{sc})/2C_{\mathrm{dc}} \\ V_n(k+1) = V_n(k) \\ -T_s(\left|S_{a1} - S_{a3}\right| i_{sa} + \left|S_{b1} - S_{b3}\right| i_{sb} \\ + \left|S_{c1} - S_{c3}\right| i_{sc})/2C_{\mathrm{dc}} \end{cases}. \tag{16}$$

As shown in (16), the currents across DCVs are obtained in terms of switching states and output currents. Hence, measuring dc-link capacitor currents is avoided.

B. MPC Algorithm Without Weighting Factors

Three targets are required to be achieved for the 3P-5L-ANPC. They include tracking current references, balancing FCVs, and balancing DCVs. Therefore, the cost function can be selected as

$$\begin{aligned} J_c = {} & \sum_{x=a,b,c} \left|i^*_{sx}(k+1) - i_{sx}(k+1)\right| \\ & + \lambda_{v1} \sum_{x=a,b,c} \left|V^*_{fx}(k+1) - V_{fx}(k+1)\right| \\ & + \lambda_{v2} \left(\left|V_p(k+1) - V_n(k+1)\right|\right) \end{aligned} \tag{17}$$

where superscript * means the reference of control variables. λ_{v1} and λ_{v2} represent weighting factors.

The cost function (17) consists of three terms. The first term penalizes the error between the current reference and the predicted current. The second and third terms penalize the FCV error and the DCV error, respectively.

In terms of (6), (7), (10), (16), and (17), one switching state that minimizes the cost function (17) is selected as the optimal switching state. For the conventional VSF MPC, this requires the prediction of three-phase currents, three FCVs, and two DCVs. Besides, all the 512 switching states need to be iteratively evaluated online, which is computationally intensive. Furthermore, there is only one switching state operation per control cycle, resulting in a VSF.

To lessen the computational burden, the cost function (17) can be modified on the basis of voltage model. Thus, it is rewritten as

$$\begin{aligned} J_v = {} & \sum_{x=a,b,c} \left|V^*_{xn}(k) - V_{xn}(k)\right| \\ & + \lambda_1 \sum_{x=a,b,c} \left|V^*_{xf}(k+1) - V_{xf}(k+1)\right| \\ & + \lambda_2 \left(\left|V_p(k+1) - V_n(k+1)\right|\right) \end{aligned} \tag{18}$$

where λ_1 and λ_2 are weighting factors for balancing FCVs and DCVs, respectively. The desired output voltage V^*_{xn} is derived from (1)

$$V^*_{xn}(k) = Ri_{sx}(k) + L[i^*_{sx}(k+1) - i_{sx}(k)]/T_s\ \ (x = a, b, c) \tag{19}$$

where $i^*_{sx}(k+1)$ $(x = a, b, c)$ means the output current reference at the $(k+1)$th instant.

From (18), it can be found that two weighting factors are required to be tuned. The first control objective is to ensure output current reference tracking. The second and third control objectives are to balance FCVs and DCVs, respectively. Weighting factors λ_1 and λ_2 indicate the relative importance of the second and third control objectives, respectively. λ_1 and λ_2 can be adjusted to realize the desired performance. Thus, it is highly desirable to eliminate the weighting factors for the simplification of MPC for 3P-5L-ANPC. The cost function that eliminates the weighting factors can be expressed as

$$J_V = \sum_{x=a,b,c} \left|V^*_{xn}(k) - V_{xn}(k)\right|. \tag{20}$$

The cost function (20) only selects voltage vectors to track current references, and it does not consider balancing FCVs and DCVs. The balancing of FCVs and DCVs is realized by choosing redundant switching states.

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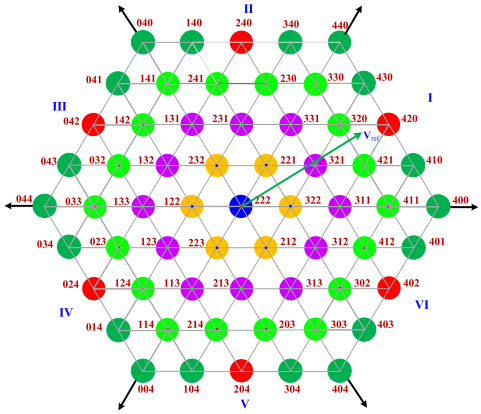


Fig. 3. Sixty-one voltage vectors with reduced CMV.

TABLE II
VOLTAGE VECTORS SELECTION

First-stage selected voltage vectors	Second-stage candidate voltage vectors
(420)	(222),(322),(311),(411),(400),(221),(321),(421),(410),(331),(320),(420),(330),(430),(440)
(240)	(222),(221),(331),(330),(440), (232),(231),(230),(340),(131),(241),(240),(141),(140),(040)
(042)	(222),(232),(131),(141),(040), (122),(132),(142),(041),(133),(032),(042),(033),(043),(044)
(024)	(222),(122),(133),(033),(044), (223),(123),(023),(034),(113),(124),(024),(114),(014),(004)
(204)	(222),(223),(113),(114),(004), (212),(213),(214),(104),(313),(203),(204),(303),(304),(404)
(402)	(222),(212),(313),(303),(404), (322),(312),(302),(403) ,(311),(412),(402),(411),(401),(400)

As shown in (20), for the conventional MPC approach, there are 125 (5^3) voltage vectors taking part in MPC optimization, which is time-consuming. Besides, it is paramount to reduce the CMV for a multilevel converter. Large CMVs will produce high bearing currents when the converter is applied in a motor drive system, resulting in high conducted and radiated electromagnetic interference. According to the CMV definition in (5), the CMV ranges from $-V_d/2$ to $V_d/2$ for the total 125 voltage vectors. To reduce the CMV, only 61 voltage vectors among the total 125 voltage vectors should be considered in the MPC optimization. The selected 61 voltage vectors are displayed in Fig. 3 in the stationary $\alpha\beta$ reference frame, which illustrates the CMV of the six voltage vectors "400," "440," "040," "044," "004," and "404" ranging from $-V_d/3$ to $V_d/3$, and the CMV of other 56 voltage vectors ranges from $-V_d/6$ to $V_d/6$.

To reduce the computational burden, a three-stage MPC for the 3P-5L-ANPC is proposed. The first stage chooses one of the medium voltage vectors ("**420**," "**240**," "**042**," "**024**," "**204**," "**402**") with red color shown in Fig. 3, which minimizes cost function (18). After obtaining the optimal medium voltage vector, those voltage vectors in the same sector with the optimal medium voltage vector will be evaluated in MPC optimization in the second stage. Various voltage vectors participating in the second stage of the proposed MPC are listed in Table II. Finally, the third stage is to choose proper redundant switching states to balance FCVs and DCVs.

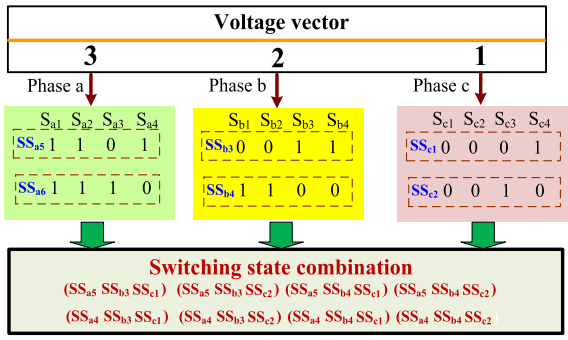


Fig. 4. Switching state combination of the voltage vector (321).

As listed in Table II, it can be observed that the number of candidate voltage vectors is greatly decreased from 61 to 21 (six candidate voltage vectors in the first stage and 15 candidate voltage vectors in the second stage). Thus, the computational efficiency has been significantly improved for the presented MPC.

C. Balancing Capacitor Voltages

As listed in Table II, 15 voltage vectors need to be evaluated in stage two of MPC optimization per control cycle. For each voltage vector, the redundant switching states are explored to control FCVs and DCVs. Taking the voltage vector (321) as an example, there are two switching combinations for each phase. Thus, there are eight (2^3) switching state combinations in total, which is depicted in Fig. 4.

To effectively control FCVs, a function G in the light of the FC energy deviation is constructed as

$$G = \sum_{x=a,b,c} C_x (V_{fx} - V_d/4)^2/2 \;\; x = a, b, c. \tag{21}$$

To balance FCVs, the function G should be minimized. Thus, the following condition should be satisfied:

$$\frac{dG}{dt} = C_x (V_{fx} - V_d/4) \frac{dV_{fx}}{dt} \leq 0 \;\; x = a, b, c. \tag{22}$$

Substituting (10) into (22), it yields

$$(V_{xf} - V_d/4)(S_{x3} - S_{x4}) i_{sx} \leq 0 \;\; x = a, b, c. \tag{23}$$

For the phase-a FC, switching states $\mathbf{SS_{a1}}$ and $\mathbf{SS_{a2}}$, $\mathbf{SS_{a5}}$ and $\mathbf{SS_{a6}}$ produce the same output voltage but opposite effects on FCs according to Table I. Therefore, $\mathbf{SS_{a1}}$ ($\mathbf{SS_{a2}}$) and $\mathbf{SS_{a5}}$ ($\mathbf{SS_{a6}}$) are considered as redundant switching states. When the output voltage is $V_d/4$ or $-V_d/4$, the redundant switching states satisfying (23) are chosen and utilized during the next control cycle. For example, assume the FCV V_{fa} is more than $V_d/4$ with generating $V_d/4$ voltage, $\mathbf{SS_{a5}}$ is chosen when the phase-a output current is more than zero, and *vice versa*.

Similarly, DCVs are also balanced via utilizing proper redundant switching states. The deviation of the NP voltage can be defined as

$$\Delta V_O = V_n - V_p. \tag{24}$$

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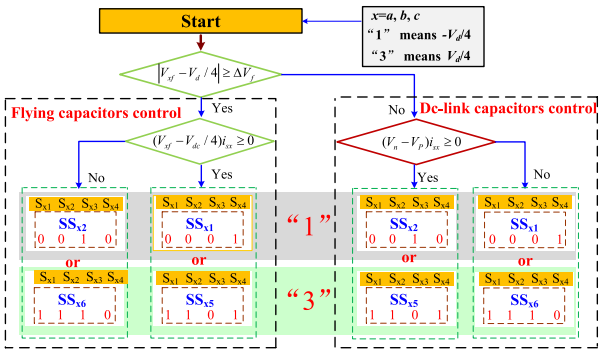


Fig. 5. Control strategy of balancing capacitor voltages.

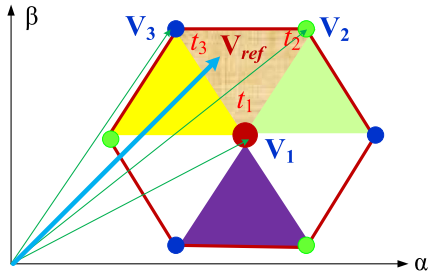


Fig. 6. Principle of conventional SVPWM techniques.

From Table I, at the output voltage $V_d/4$, $\mathbf{SS_{a5}}$ will affect ΔV_o. However, the corresponding redundant switching state $\mathbf{SS_{a6}}$ has no effect on the DCVs. As displayed in Fig. 1, each phase FCV only depends on the corresponding switching states of that phase. And switching states of phases b and c cannot influence the FCV of phase a. In addition, for the DCVs, three phases share the same dc-link bus and NP. It means each phase will contribute to the balance of DCVs. Therefore, for each phase of the 3P-5L-ANPC, the regulation of its FCV is given a higher control priority than that of the DCV. When the FCV is kept within the allowable range, the proper switching states are chosen to balance DCVs. On the basis of the above analysis, the control strategy for balancing DCVs and FCVs at the same time is shown in Fig. 5.

The allowable fluctuation of the FCV ΔV_f is a very important parameter, which directly influences the performance of balancing FCVs. Generally, it is selected as the range from 3% to 10% of the rated voltage. In the system, ΔV_f is set to 5 V in experiment evaluation.

D. FSF MPC Algorithms

For conventional SVPWM techniques, multiple voltage vectors are applied during each control cycle, which achieves FSF. The basic principle of SVPWM is shown in Fig. 6.

For the conventional SVPWM, the voltage reference $\mathbf{V}_{\text{ref}}$ is synthesized by the nearest three voltage vectors and satisfies as follows:

$$\begin{cases} \mathbf{V}_{ref}T_s = \mathbf{V}_1 t_1 + \mathbf{V}_2 t_2 + \mathbf{V}_3 t_3 \\ t_1 + t_2 + t_3 = T_s \end{cases} \tag{25}$$

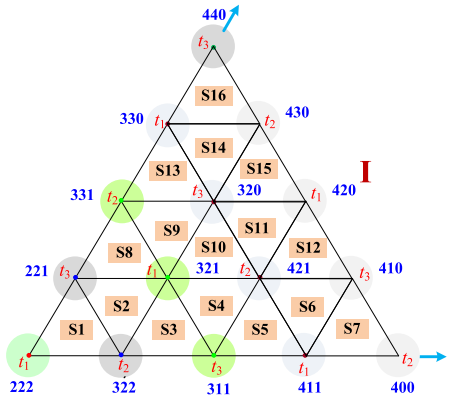


Fig. 7. Duration times in the large sector I.

where t_x $(x = 1, 2, 3)$ represents the duration time of the voltage vector $\mathbf{V}_x$ $(x = 1, 2, 3)$.

The implementation of FSF MPC algorithm refers to the SVPWM approach, which achieves three voltage vectors action per control cycle. The first step is to determine candidate voltage vectors near to the voltage reference $\mathbf{V}_{\text{ref}}$. The second step is to determine the duration times of distinct voltage vectors based on their resultant cost function values. A larger value of the cost function implies smaller duration time for a certain voltage vector and *vice versa*. Suppose the cost function values for $\mathbf{V}_1$, $\mathbf{V}_2$, and $\mathbf{V}_3$ are J_1, J_2, and J_3, respectively. Then, the duration times can be calculated as

$$\begin{cases} t_1 = T_s K/J_1 & 0 \le t_1 \le T_s \\ t_2 = T_s K/J_2 & 0 \le t_2 \le T_s \\ t_3 = T_s K/J_3 & 0 \le t_3 \le T_s \\ T_s = t_1 + t_2 + t_3 \end{cases} \tag{26}$$

where K is a constant and larger than zero. Solving (26) and eliminating the coefficient K, the duration times are derived as

$$\begin{cases} t_1 = \frac{T_s J_2 J_3}{J_1 J_2 + J_2 J_3 + J_1 J_3} & 0 \le t_1 \le T_s \\ t_2 = \frac{T_s J_1 J_3}{J_1 J_2 + J_2 J_3 + J_1 J_3} & 0 \le t_2 \le T_s \\ t_3 = \frac{T_s J_1 J_2}{J_1 J_2 + J_2 J_3 + J_1 J_3} & 0 \le t_3 \le T_s \\ T_s = t_1 + t_2 + t_3 \,. \end{cases} \tag{27}$$

In terms of (8) and (19), the cost function values of J_1, J_2, and J_3 in (20) can be obtained. The small triangular sector cost function can be obtained for the duration time calculation of distinct voltage vectors and the expression is shown as

$$J_s = \frac{t_1}{T_s} J_1 + \frac{t_2}{T_s} J_2 + \frac{t_3}{T_s} J_3. \tag{28}$$

As shown in Fig. 7, there are 16 small triangular sectors in sector I. According to (27), the time duration of each voltage vector for different triangular sectors in sector I can be calculated. Then, according to (28), each triangular sector cost function is obtained and denoted as $J_{s1}, J_{s2}, J_{s3}, \ldots, J_{s16}$. One of 16 triangular sector cost functions with the minimum cost function is chosen as the best triangular sector and corresponding voltage vectors and switching sequences will be applied in the next sampling period.

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TABLE III
SWITCHING SEQUENCES IN DIFFERENT SMALL TRIANGULAR SECTORS IN LARGE SECTOR 1

Small sectors	Switching sequences
S1	221-222-322-222-221
S2	221-321-322-321-221
S3	311-321-322-321-311
S4	311-321-421-321-311
S5	311-411-421-411-311
S6	410-411-421-411-410
S7	400-410-411-410-400
S8	221-321-331-321-221
S9	320-321-331-321-320
S10	320-321-421-321-320
S11	320-420-421-420-320
S12	410-420-421-420-410
S13	320-330-331-330-320
S14	320-330-430-420-320
S15	320-420-430-420-320
S16	330-430-440-430-330

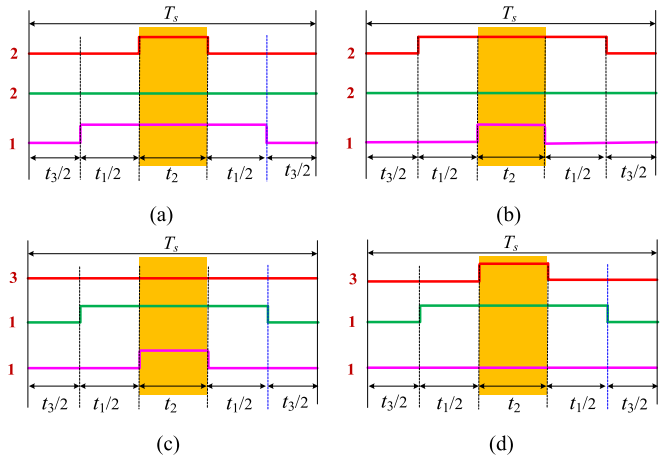


Fig. 8. Switching sequences and duration times. (a) Small sector S1. (b) Small sector S2. (c) Small sector S3. (d) Small sector S4.

Duration times of different voltage vectors in the large sector I are shown in Fig. 7. The large sector I can be divided into 16 small triangular sectors denoted as "S1," "S2," "S3," "S4," …"S16." Switching sequences of each small triangular sectors are listed in Table III. As can be seen in Table III, it has the feature that output voltage level of one phase keeps unchanged, resulting in the reduced switching frequency. On the basis of (19), (27), and (28), the duration times and the sector cost function can be obtained. The duration times and switching sequences in the small triangular sectors S1, S2, S3, and S4 are displayed in Fig. 8. Similarly, other small triangular sectors in the large sector I and other large sectors can be obtained. As shown in Fig. 8(a), the duration time is t_3 for the voltage vector 221, which illustrates that the phase-c output level of the 3P-5L-ANPC is "1." Then, it can be utilized to balance the DCVs and FCVs during the t_3 time in Fig. 8. Similarly, the duration time is t_2 when the voltage

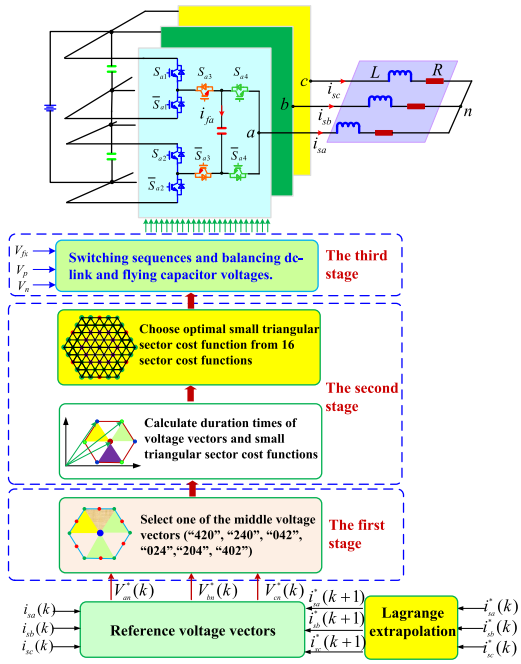


Fig. 9. Controls strategy for the 3P-5L-ANPC.

vector 322 is applied in the 3P-5L-ANPC, which means the phase-a output level is "3." The output level "3" can be adopted to control capacitor voltages of the 3P-5L-ANPC according to Fig. 5.

As analyzed above, the proposed MPC control strategy is summarized in Fig. 9. It simultaneously achieves multiobjectives including the improved computation efficiency, reduced CMV, DCVs and FCVs balancing, and FSF control without weighing factors.

As depicted in Fig. 9, the proposed MPC is implemented through three stages. The first one selects an optimal medium voltage vector that minimizes the cost function (20). Then, those voltage vectors in the same sector will be involved in the MPC optimization. The second stage calculates the duration times for three voltage vectors according to (27) and the small triangular sector cost function in (28). Then, the small triangular sector with the minimal cost function (28) will be obtained and the corresponding duration times can be calculated. The third stage balances DCVs and FCVs by selecting proper redundant switching states.

IV. EXPERIMENTAL EVALUATIONS

To demonstrate the feasibility of the proposed MPC algorithm, steady-state and dynamic experimental tests have been carried out. The down-scale laboratory platform is established and shown in Fig. 10. For the 3P-5L-ANPC platform, the floating-point dual-core DSP (TMS320F28377D) is used to implement the proposed MPC algorithm. The field programmable gate array of Cyclone IV EP4CE115F29C7N is utilized to generate 24 PWM signals. Table IV reveals the main experimental parameters, and Table V shows different experimental conditions.

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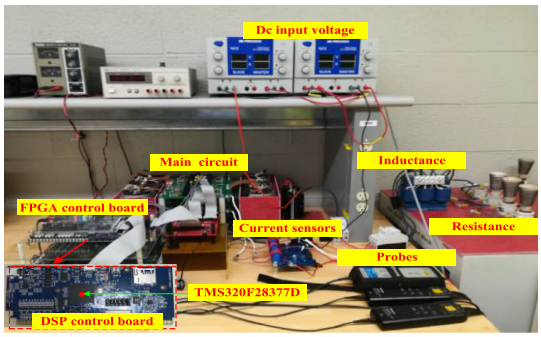


Fig. 10. Laboratory platform.

TABLE IV
MAIN SYSTEM PARAMETERS

Parameter	Description	Experiment
V_d	DC-bus voltage	200 V
C_{dc}	DC-link voltage capacitors	1000 μF
C_{af}, C_{bf}, C_{cf}	Flying capacitors	500 μF
L	Filter inductance	5 mH
R	Load resistance	18 Ω
f_s	Sampling frequency	10 kHz
ΔV_f	Allowable fluctuation	5 V

TABLE V
EXPERIMENTAL TEST CONDITIONS

Conditions	Current amplitude reference	Current frequency reference
Case 1	4 A	50 Hz
Case 2	4 A	10 Hz
Case 3	From 2 A to 4 A	50 Hz
Case 4	From 4 A to 2 A	50 Hz
Case 5	4 A	From 50 Hz to 100 Hz
Case 6	4 A	From 50 Hz to 25 Hz

TABLE VI
EXECUTION TIME COMPARISION

Algorithms	Measurement and Initialization Time	MPC Implementation	Total Time
Conventional FSF MPC	5.8 μs	191.1 μs	196.9 μs
Proposed MPC	5.8 μs	41.8 μs	47.6 μs

A. Execution Time Evaluation

The computational burden is considered as one of the main concerns for MPC algorithms. The conventional FSF MPC first evaluate 96 small triangle sectors, then, the small triangle sector with minimum cost function is selected as the optimal triangle sector. The corresponding voltage vectors will be applied in the next control cycle. Table VI lists the execution time when both MPC algorithms are implemented by DSP TMS320F28377D. In Table VI, both the measurement and initialization time such as the A/D sampling, initialization of key variables, and other tasks are included. As seen from Table VI, the execution time of the proposed MPC is 41.8 μs while the conventional FSF MPC requires 191.1 μs. The execution time of the proposed MPC is only 21.8% of the conventional FSF MPC, which greatly improves the computational efficiency of MPC algorithms for the 3P-5L-ANPC application.

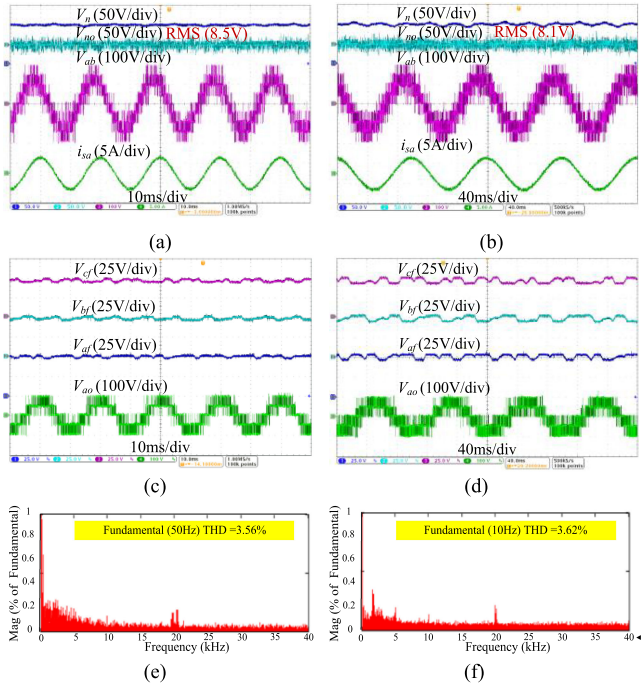


Fig. 11. Steady-state experimental results in Case 1 and Case 2. (a), (c), and (e) in Case 1. (b), (d), and (f) in Case 2.

B. Steady-State Experimental Evaluation

Fig. 11 displays the steady-state experimental waveforms. Two different frequencies, 50 and 10 Hz, are examined in Case 1 and Case 2, respectively. The waveforms in each figure show the CMV (V_{no}), output line–line voltage (V_{ab}), phase-a output current (i_{sa}), three-phase FCVs (V_{af}, V_{bf}, V_{cf}), phase-a output voltage (V_{ao}), and the frequency spectrum of the output current, respectively. As shown in Fig. 11, it can be summarized as follows.

1) The output line–line voltage has nine output steps and the phase voltage is five steps, which verify the five-level output voltage of the 5L-ANPC.
2) The output current is sinusoidal with the high-quality waveshape. The total harmonic distortion (THD) is 3.56% in Case 1 and 3.62% in Case 2. Furthermore, high-order harmonics of output currents mainly concentrate on the multiple time of the sampling frequency, such as 10 and 20 kHz. Thus, the FSF is achieved, which can benefit the load filter design.
3) The proposed MPC algorithm can effectively reduce the CMV of the 3P-5L-ANPC since the measured root mean square values of the CMV are 8.5 and 8.1 V in Case 1 and Case 2, respectively.
4) The dc-link lower capacitor voltage is well controlled around 100 V (V_d/2). The peak-to-peak ripple of the lower DCVs are 6 and 9 V in Case 1 and Case 2, respectively. The peak–peak ripple of the lower capacitor voltage

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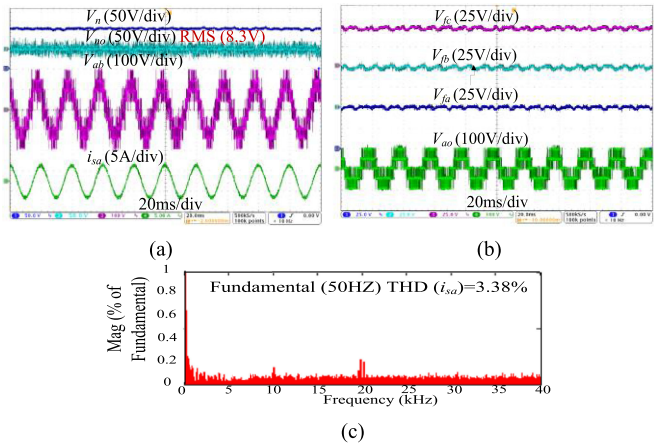


Fig. 12. Steady-state experimental results in Case 1 for the conventional SVPWM. (a) Experimental waveforms of V_n, V_{no}, V_{ab}, and i_{sa}. (b) Experimental waveforms of FCVs and V_{no}. (c) Frequency spectrum of i_{sa}.

becomes larger due to longer charging/discharging time once the output frequency becomes lower.

5) FCVs are effectively controlled at 50 V (V_{dc}/4). The peak-to-peak ripple is less than 9 V.

Therefore, the steady-state experimental results illustrate that the proposed MPC algorithm owns high-quality output voltage and current waveshapes at the steady-state conditions. Both DCVs and FCVs are well stabilized at their rated voltages with small voltage ripples.

Fig. 12 depicts the steady-state experimental results for the conventional SVPWM in Case 1. Compared to the steady-state experimental results shown in Fig. 11 for the proposed MPC algorithm, it can be clearly observed that steady-state performance for the proposed MPC and the conventional SVPWM approach is very similar. However, the proposed MPC algorithm avoids selecting PI parameters by trial-and-error.

C. Dynamic Experimental Evaluation

The dynamic performance of the proposed MPC is evaluated in Case 3 to Case 6, which includes the output current amplitude and frequency step change. Figs. 13 and 14 show the corresponding experimental results. It can be clearly observed as follows.

1) The 5L-ANPC takes approximately 1 ms to reach the reference when the amplitude/frequency step change happens.
2) The DCVs and FCVs are well controlled at the rated value without any instability issue during the dynamic process.

From the dynamic experimental results, it can be concluded that the proposed MPC method provides fast and robust dynamic response when the large current change happens. Besides, it realizes strong dynamic balancing capability of DCVs and FCVs, which can significantly enhance the 5L-ANPC's reliability.

Fig. 15 depicts the dynamic experimental results for the conventional MPC proposed in [42], which utilizes one voltage vector in every control cycle and results in VSF performance.

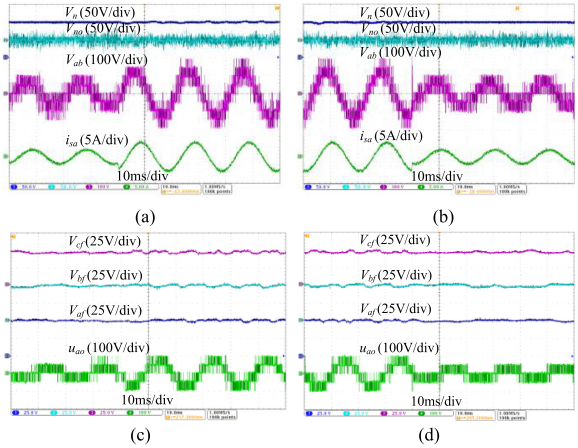


Fig. 13. Dynamic experimental results in Case 3 and Case 4. (a) and (c) in Case 3. (b) and (d) in Case 4.

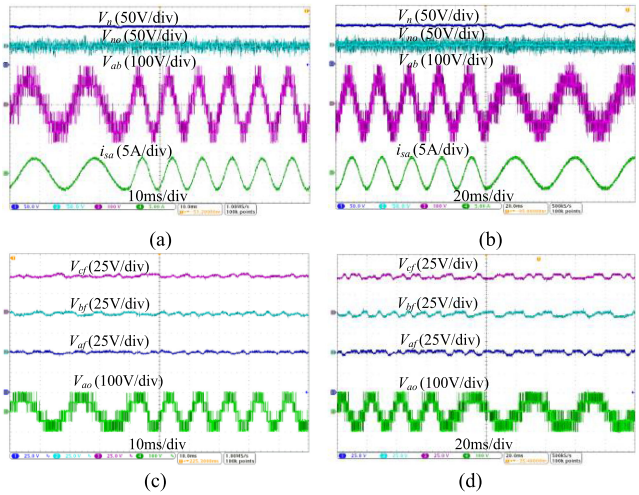


Fig. 14. Dynamic experimental results in Case 5 and Case 6. (a) and (c) in Case 5. (b) and (d) in Case 6.

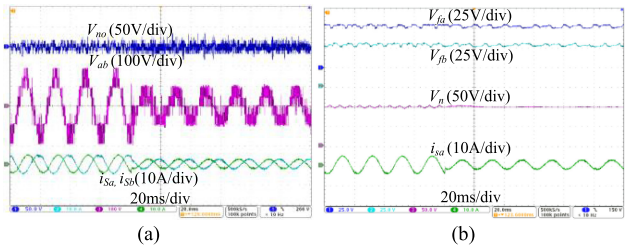


Fig. 15. Dynamic experimental results of the conventional MPC in [42] in Case 4. (a) Experimental waveforms of V_{no}, V_{ab}, i_{sa}, and i_{sb}. (b) Experimental waveforms of V_{fa}, V_{fb}, V_n, and i_{sa}.

Compared to the dynamic response of the proposed MPC algorithm shown in Fig. 13, it can be observed that both MPC algorithms have almost similar dynamic response.

D. Parameter Sensitivity Evaluation

In the practical system, the real inductance L_r will change under different operation conditions. The MPC algorithm should

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TABLE VII
PARAMETER SENSITIVITY OF ΔL

	ΔL				
	-30%	-10%	0%	+10%	+30%
THD	4.54%	3.80%	3.56%	3.42%	3.07%
$\Delta Vf_{\text{p-p}}$	9.4 V	9.1 V	9.0 V	8.8 V	8.6 V
$\Delta Vd_{\text{p-p}}$	6.3 V	6.1V	6.0 V	5.8 V	5.7 V

TABLE VIII
PARAMETER SENSITIVITY OF ΔR

	ΔR				
	-15%	-5%	0%	+5%	+15%
THD	3.10%	3.32%	3.56%	3.63%	3.85%
$\Delta Vf_{\text{p-p}}$	10.8 V	9.7 V	9.0 V	7.5 V	5.7 V
$\Delta Vd_{\text{p-p}}$	6.6 V	6.2 V	6.0 V	5.5 V	4.8 V

be robust for the inductance change. The variation percent ΔL of the inductance is defined as

$$\Delta L = \frac{L_r - L_m}{L_m} \times 100\% \tag{29}$$

where L_m means the model inductance and is considered as a constant $L_m = 5$ mH in implementing MPC algorithms.

Similarly, the real resistance load R_r changes under different operation conditions and the variation percent ΔR of the resistance load is defined as

$$\Delta R = \frac{R_r - R_m}{R_m} \times 100\% \tag{30}$$

where R_m means the model resistance load and is kept constant $R_m = 18\ \Omega$ in implementing MPC algorithms.

Tables VII and VIII list the THD of the phase-a current, the peak–peak ripple of the phase-a FCV ($\Delta Vf_{\text{p–p}}$), and the peak–peak ripple of the DCV ($\Delta Vd_{\text{p–p}}$) for the proposed FSF MPC in Case 2 with changing ΔL and ΔR, respectively. As listed in Tables VII and VIII, it can be observed as follows.

1) Although the THD decreases with respect to the variation percent ΔL, however, the THD change is less than 5% when the ΔL changes from –30% to +30%.
2) Both $\Delta Vf_{\text{p–p}}$ and $\Delta Vd_{\text{p–p}}$ are basically unchanged even when the variation percent ΔL is high up to 30% of the rated inductance.
3) The THD is basically unchanged when the ΔR changes from –15% to +15%.

Thus, it can be concluded that the variations of the inductance and the resistance load have little influence on the steady-state performance, which verifies that the proposed FSF MPC algorithm has strong robustness.

VI. CONCLUSION

Three-stage MPC with FSF for a 3P-5L-ANPC has been proposed in the article. Verified by the extensive experimental results, the following conclusions can be summarized.

1) It adopts three stages to implement the proposed MPC algorithm and the execution time of the proposed MPC is only 21.8% of the conventional FSF MPC, which greatly improves the computational efficiency of MPC algorithms.
2) The high-order harmonics are concentrated on the multiple time of the sampling frequency, such as 10 and 20 kHz. Thus, it achieves FSF control of the 3P-5L-ANPC like the SVPWM method, which is beneficial for the load filter design.
3) The 3P-5L-ANPC achieves high-quality output voltage and current waveshapes, reduced CMV, and well-balanced DCVs and FCVs during the steady-state condition. The THD value of outputs is less than 5% with good steady-state performance.
4) The converter realizes fast and robust dynamic response in terms of current tracking and capacitor balancing. Especially, DCVs and FCVs can be actively recovered to the rated voltage when the large voltage deviation happens.

Thus, the proposed MPC algorithm for the 3P-5L-ANPC has simultaneously achieved multiple objectives including current reference tracking, DCVs and FCV balancing, reduced CMV, and FSF function. It can significantly enhance the reliability and performance of the 3P-5L-ANPC for high-power applications.

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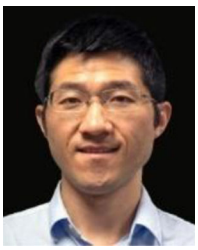
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